ESS Technology, Inc.

Swan-2™ ES4318
DVD Processor Chip
Data Sheet

OVERVIEW

The Swan-2™ ES4318 Processor is a single-chip solution for a Digital Versatile Disc (DVD) player that integrates MPEG video decoding, DVD system navigation, Content Scrambling System (CSS), and Dolby™ Digital (AC-3) and MPEG audio decoding. The fully programmable Swan-2™ ES4318 is based on a proprietary ESS architecture. It offers the best feature set in comparison to any currently existing DVD chip, and a glueless interface to various peripheral components. The Swan-2™ ES4318 is the most cost effective solution in its class with an integration level and quality that set new benchmarks.

The Swan-2™ ES4318 processor is capable of decoding Dolby™ Digital (AC-3) or DTS digital surround, simultaneously with MPEG-1 or MPEG-2 video. For embedded applications, the Swan-2™ ES4318's internal RISC processor can be used in place of a microcontroller to provide all system control, DVD system navigation, CSS decryption, and many other features. On-chip, multi-tap filters provide arbitrary scaling with state of the art SmartScale™ technology useful for video standards conversion. SmartStream™ technology from ESS provides video error concealment and video post-processing, leading to the highest playability and video quality. Other features included in the Swan-2™ ES4318 are video letterbox display, DVD Sub-Picture overlay, and On-Screen Display.

The ES4318 provides a glueless 8/16-bit parallel interface to most DVD servo/loaders. It connects directly with 8/16-bit ROM and 16-bit SDRAM/EDO. An 8-bit YUV video interface supports many TV encoders. General purpose auxiliary pins are provided to control various peripheral devices. A standard I^2S interface supports popular audio DACs and ADCs. The ES4318 also features a direct S/PDIF output. Figure 1 shows a block diagram of a typical stand-alone system using the Swan-2™ ES4318 with the glueless SDRAM interface.

The DVD system stream from a DVD disc is passed to the Swan-2™ ES4318 through the 8-bit/16-bit parallel host interface. The Swan-2™ ES4318 parses the system layer and demultiplexes the audio and video streams. Audio is decoded and passed through the I^2S audio serial bus to an external audio DAC and then to the speakers. Video is decoded and output as YUV pixels to an NTSC or PAL video encoder. System control and housekeeping functions (keypad and remote control) are also provided on-chip.

FEATURES

- Single-Chip DVD video decoder in a 208-pin PQFP package
- Supports MPEG-1 system and MPEG-2 program streams
- Programmable multimedia processor architecture
- Compatible with Audio CD, VideoCD, VCD 3.0, and Super VideoCD (SVCD)
- DVD Navigation 1
- Built-in Content Scrambling System (CSS)

Video

- Pan & Scan and Letter-Box conversions
- Trick modes include Slow, Fast Forward, Fast Reverse, Step, and Goto
- Sub-Picture decoder
- 4-bit On-Screen Display (OSD) with 4-bit blending
- 8-bit YUV component video output

Audio

- Built-in Karaoke key-shift function
- Dolby™ Digital 2-channel downmix audio output for Dolby™
- Dolby Pro Logic
- Linear PCM streams for 24 bit/96KHz
- Concurrent S/PDIF out and 2-channel audio output
- Sensaura Dolby Digital Virtual Suround
- DTS Digital Surround 2-channel downmix stereo output
- S/PDIF output for encoded AC-3, DTS Digital output or Linear PCM

Peripheral

- Glueless interface to DVD loaders (ATAPI or A/V bus I/F)
- Bidirectional I^2S audio interface
- Direct servo/loader interface
- 8 general-purpose auxiliary ports
- Single 27 MHz clock input

Smart Technology

- SmartZoom™ for motion zoom & pan
- SmartScale™ for NTSC to PAL conversion and vice versa
- SmartStream™ for video error concealment

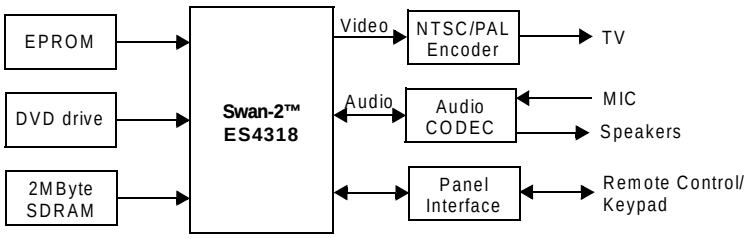

Figure 1 Typical Swan-2™ ES4318 System Block Diagram.

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FIGURES

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SWAN-2™ ES4318 PINOUT DIAGRAM

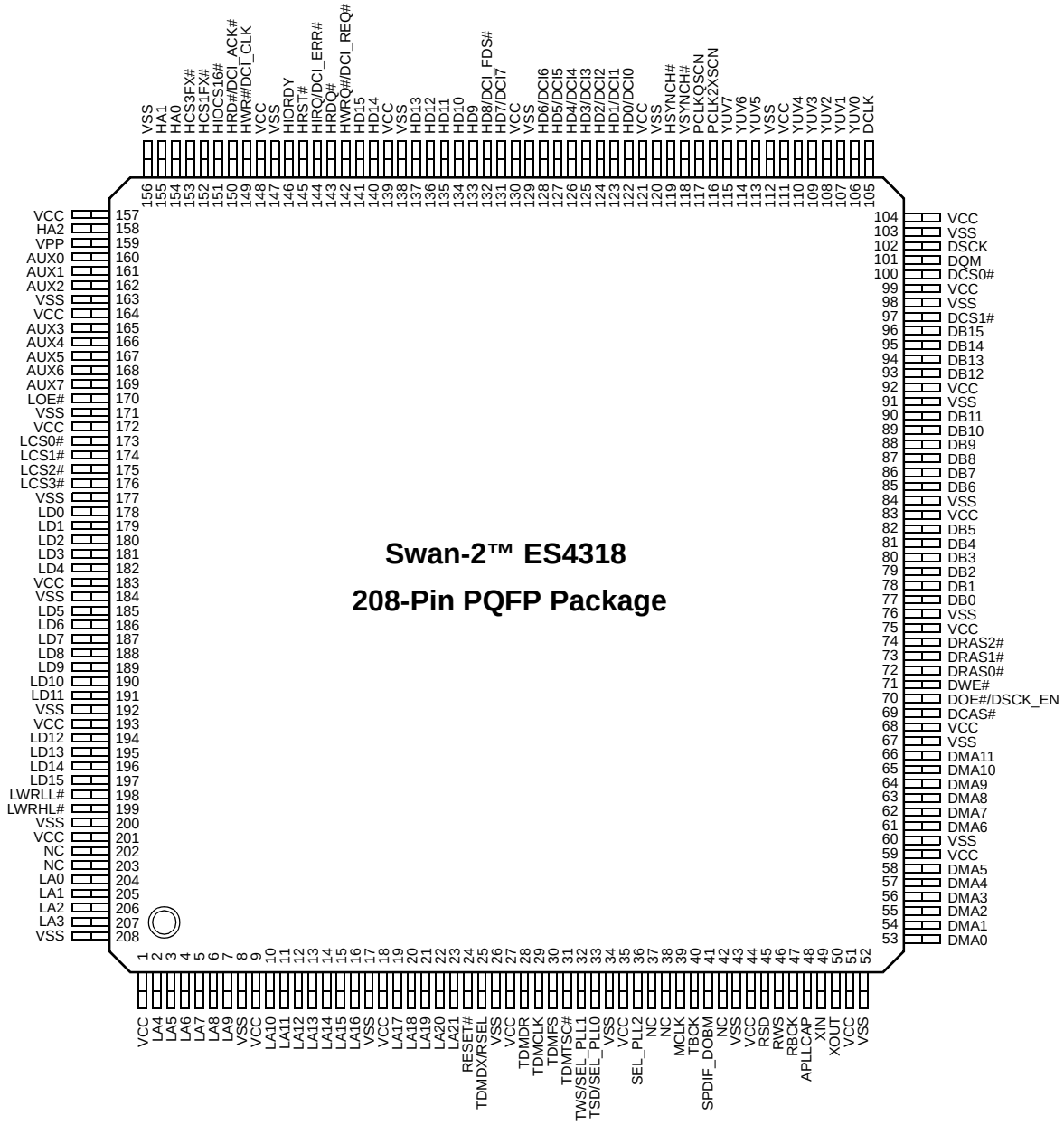
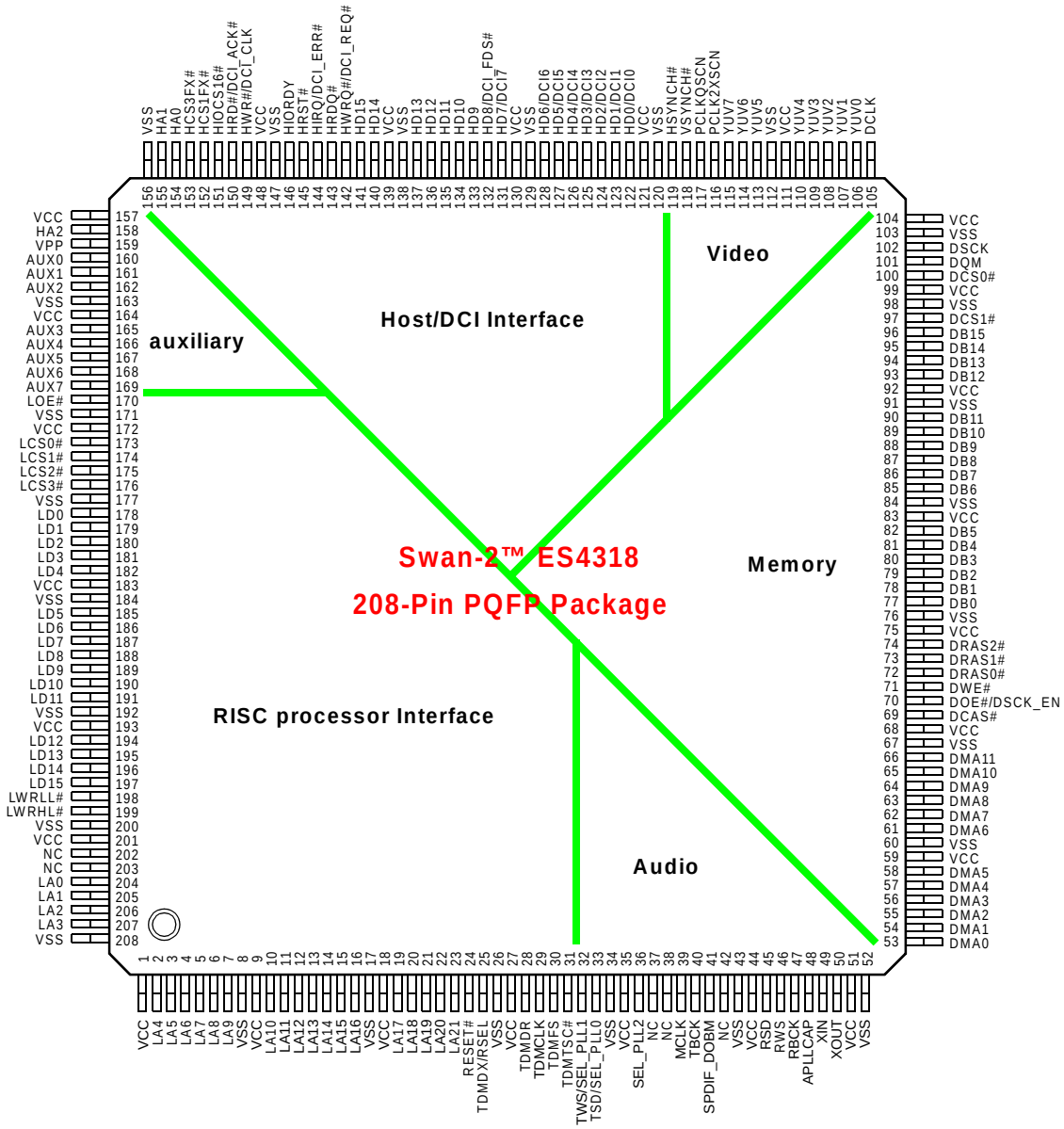


Figure 2 Swan-2™ ES4318 Pinout

PIN GEOGRAPHY



SWAN-2™ ES4318 PIN DESCRIPTION

Name	Number	I/O	Definition
VCC	1, 9, 18, 27, 35, 44, 51, 59, 68, 75, 83, 92, 99, 104, 111, 121, 130, 139, 148, 157, 164, 172, 183, 193, 201	I	3.65 V ± 150 mv.
LA[21:0]	23:19,16:10,7:2,207:204	O	Device address output.
VSS	8,17,26,34,43,52,60,67,76,84,91,98,103,112,120,129,138,147,156,163,171,177,184,192,200,208	I	Ground.
RESET#	24	I	Reset input, active low.
TDMDX	25	O	TDM transmit data.
RSEL		I	ROM Select **RSEL** **Selection** 0 16-bit ROM 1 8-bit ROM
TDMDR	28	I	TDM receive data.
TDMCLK	29	I	TDM clock input.
TDMFS	30	I	TDM frame synch.
TDMTSC#	31	O	TDM output enable, active low.
TWS	32	O	Audio transmit frame sync.
SEL_PLL1		I	Select PLL1.
TSD	33	O	Audio transmit serial data port.
SEL_PLL0		I	Select PLL0. **SEL_PLL2** **SEL_PLL0** **Clock Output** 0 0 2.5 x DCLK 0 1 3 x DCLK 1 0 3.5 x DCLK 1 1 4 x DCLK
SEL_PLL2	36		Select PLL2. See the table for pin number 33.
MCLK	39	I/O	Audio master clock for audio DAC.
TBCK	40	I/O	Audio transmit bit clock.
SPDIF_DOBM	41	O	S/PDIF (IEC958) Format Output.
RSD	45	I	Audio receive serial data.
RWS	46	I	Audio receive frame synch.
RBCK	47	I	Audio receive bit clock.
APLLCAP	48	I	Analog PLL Capacitor.
XIN	49	I	Crystal input.
XOUT	50	O	Crystal output.
DMA[11:0]	66:61,58:53	O	DRAM address bus.
DCAS#	69	O	Column address strobe, active low.
DOE#	70	O	Output enable, active low.
DSCK_EN		I	Clock Enable, active low.
DWE#	71	O	DRAM write enable, active low.
DRAS[2:0]#	74:72	O	Row address strobe, active low.
DB[15:0]	96:93,90:85,82:77	I/O	DRAM data bus.
DCS[1:0]#	97,100	O	SDRAM chip select [1:0], active low.
DQM	101	O	Data input/output mask.
DSCK	102	O	Clock to SDRAM.
DCLK	105	I	Clock Input (27 MHz)
YUV[7:0]	115:113,110:106	O	8-bit YUV output.
PCLK2XSCN	116	I/O	2X pixel clock.
PCLKQSCN	117	I/O	Pixel clock.
VSYNCH#	118	I/O	Vertical synch for screen video interface, programmable for rising or falling edge, active low.
HSYNCH#	119	I/O	Horizontal sync for screen video interface, programmable for rising or falling edge, active low.
HD[15:0]	141:140,137:131,128:122	O	Host data bus
HCS1FX#	152	O	Host select 1.
HCS3FX#	153	O	Host select 3.
HIOCS16#	151	I	Device 16-bit data transfer.
HA[2:0]	158, 155:154	I/O	Host address bus.
VPP	159	I	Peripheral protection voltage. See AppNote 2.
HWR#/DCI_ACK#	149	I,I	Host write/DCI Interface Acknowledge Signal, active low.
HRD#/DCI_CLK	150	I,I	Host read/DCI Interface Clock.
HD[15:0]	141:140,137:131,128:122	I/O	Host data bus.
HWRQ#	142	O	Host write request.
HRDQ#	143	O	Host read request.
HIRQ	144	I/O	Host interrupt.
HRST#	145	O	Host reset.
HIORDY	146	I	Host I/O ready.
HWR#	149	O	Host write request.
AUX[7:0]	169:165,162:160	I/O	Auxiliary ports.
LOE#	170	O	Device output enable, active low.
LCS[3:0]#	176:173	O	Chip select [3:0], active low.
LD[15:0]	197:194, 191:185, 182:178	I/O	Device data bus.
LWRLL#	198	O	Device write enable, active low.
LWRHL#	199	O	Device write enable, active low.
NC	37,38,42,203:202		No Connect pins. Leave open.

SWAN-2™ ES4318 FUNCTIONAL DESCRIPTION

The following figure shows the internal block diagram for the Swan-2™ ES4318.

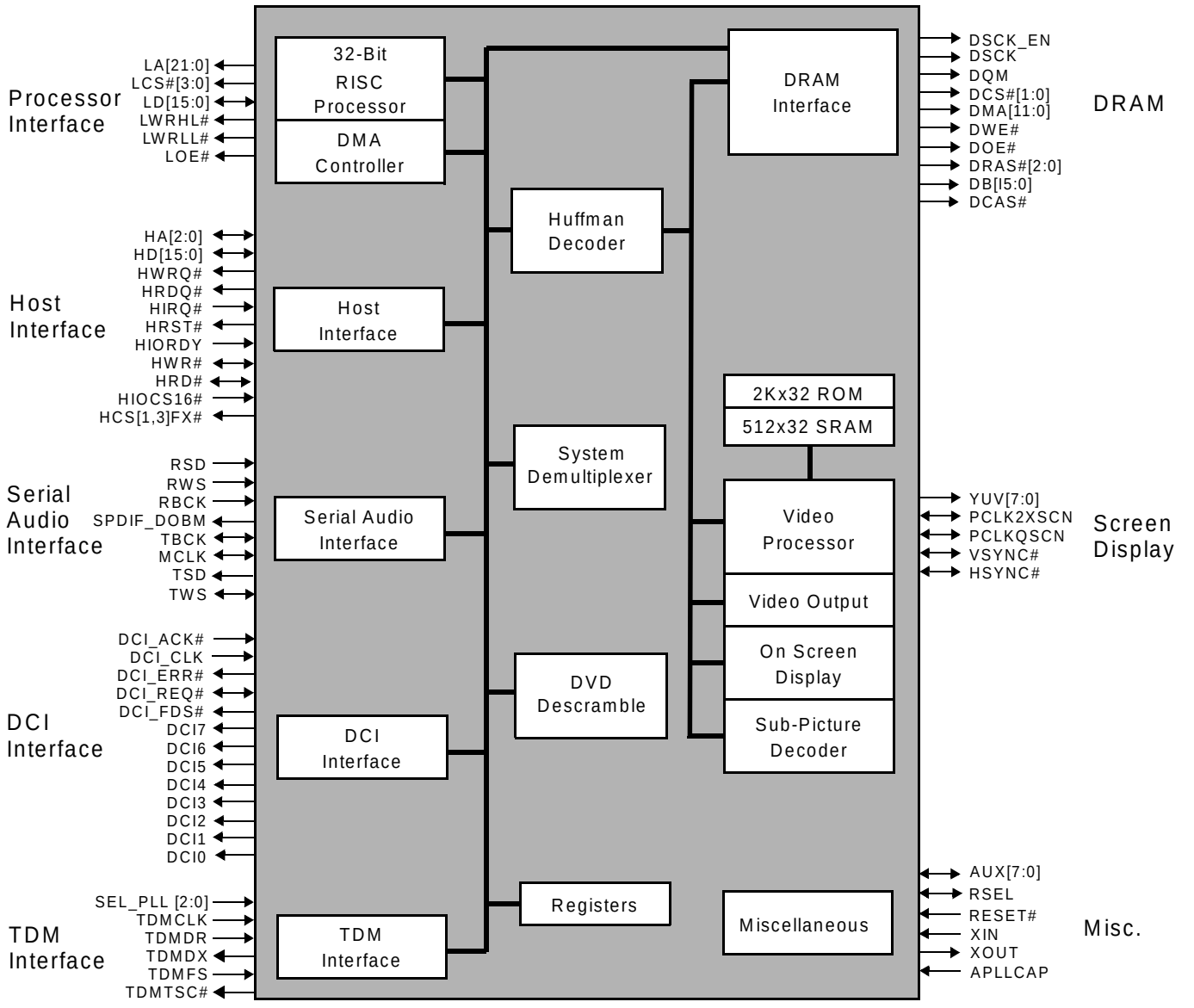


Figure 3 Swan-2™ ES4318 Block Diagram

RISC Processor

Embedded in the Swan-2™ ES4318 is a 32-bit pipelined RISC processor, with 16 Kbytes of combined instruction and data cache. Programming of the RISC processor is done mostly in C. For applications involving an external host processor the communication between a host processor and the ES4318 is handled by a host interface module as described below. The host interface can also be used for high speed data input and output.

Video Processor

The video processor consists of a programmable SIMD engine and 2 Kbytes of internal cache memory. It executes macroblock level tasks as required by the MPEG video standard. It can also be used for a wide range of time-critical signal processing tasks, such as Dolby™ Digital (AC-3) and MPEG audio decoding. It is also useful for video pre- and post-processing. It enables the Swan-2™ ES4318 to perform arbitrary vertical filtering and scaling of outgoing video. The video processor is controlled by 32-bit and 16-bit wide dual issue micro-instructions. Commonly used microcode subroutines are stored in 8 Kbytes of internal microcode ROM, while not so frequently used microcode segments can be down-loaded on demand to 2 Kbytes of internal microcode RAM.

Video Output

The video output section controls the transfer of video frames stored in the DRAM to an external TV encoder. It consists of a programmable CRT controller running in either master or slave mode.

It features display FIFOs to buffer outgoing luminance and chrominance data and performs YUV420 to YUV422 conversion. Arbitrary horizontal decimation/interpolation is achieved by a polyphase filter. Together with programmable line dropping/duplication circuitry and micro-code based post-processing running on the video processor, the Swan-2™ ES4318 is capable of arbitrating image conversion. Examples include SIF to CCIR601, Letterbox, NTSC to PAL, and PAL to NTSC conversions.

Huffman Decoder

The Huffman decoder is a high-speed engine that decodes MPEG variable length codes (VLC), using built-in MPEG-1 and MPEG-2 VLC tables. A high-level Huffman table, which controls the automatic switching from one VLC table to the next, is programmable. The input VLC data is transferred from DRAM to the Huffman decoder via a DMA channel. The resulting Zero-Run-Length-Amplitude (RLA) tokens are transferred on the DRAM bus to the video processor core.

Audio Interface

The audio interface is a bidirectional serial port that connects to an external audio ADC/DAC for the transfer of PCM (pulse coded modulation) audio data in I^2S format. It supports 16-, 24-, and 32-bit audio frames. No external master clock is required.

DRAM Interface

The Swan-2™ ES4318 provides a glueless 16-bit interface to DRAM memory chips. The maximum amount of memory supported is 8 MBytes.

This DRAM interface is configurable in depth to support 16 M-bit addressing, Extended Data Out (EDO) DRAM, and Synchronous DRAM (SDRAM). The configuration can be done in three ways:

- EDO – 256 K x 16-bit and 1 M x 16-bit
- SDRAM – 16 M-bit (512 K x 16-bit x 2 Bank), or
- A combination of EDO and SDRAM

On-Screen Display (OSD)

The video output section includes dedicated OSD hardware. The OSD operates with 2 or 4 bits per pixel palettized colors with 16 levels of transparency. It can take up the full or a partial screen area. It is multiplexed into the output video stream before Color Space Conversion (CSC) is performed. The OSD bitmap is stored in the reference DRAM.

DRAM DMA Controller

The DRAM DMA controller controls multiple DMA channels for the transfer of 16-bit data between the DRAM and the video interface, the audio interface, the Huffman decoder, the transport, the RISC processor, and the video processor. There is a separate channel for DRAM refresh.To improve DRAM bandwidth utilization, internal gateway FIFOs are used extensively.

TDM Interface

The Time Division Multiplexed (TDM) interface implements a high speed bidirectional serial bus. It can implement a number of high-speed serial protocols. The TDM interface can also act as a general-purpose 16 Mbps serial link when not constrained by TDM protocols.

Host Interface

The host interface allows communication between the RISC and an external host. It contains three ports:

- debug port (8-bit wide)
- command port (8-bit wide)
- DMA port (16-bit wide)

The host interface has two registers that control the operation of the flags and interrupts, R_HOSTRQSTAT and R_HOSTMASK for the RISC side and H_HOSTRQSTAT and H_HOSTMASK for the HOST side. Flags are used to indicate ES4318's readiness to accept or supply data over the host interface DMA channel. Interrupts may be used for exception indication from RISC-to-host or from host-to-RISC. The interrupts are maskable.

DCI Interface

In addition to TDM (serial interface) and Host (parallel interface), the Swan-2™ ES4318 offers DCI, a direct interface to DVD loaders. This 8-bit parallel interface meets the specification of many DVD loader manufacturers.

DVD Descrambling

The Swan-2™ ES4318 incorporates dedicated circuitry to perform DVD descrambling in accordance with Content Scrambling System (CSS) specification.

VIDEO INTERFACE

Video Bus

The Swan-2™ ES4318 video bus transfers digital video pixels out of the chip. In standalone applications the video bus will be connected to a monitor or an LCD panel. In workstation applications, the output bus will feed an overlay circuit so that the output video appears in a window of the Graphical User Interface (GUI).

The video bus has 8-bit YUV data pins that transfer luminance and chrominance (YUV) pixels in CCIR601 pixel format (4:2:2). In this format, there are half as many chrominance (U or V) pixels per line as luminance (Y) pixels; there are as many chrominance lines as luminance.

CRT Controller

Video output timing is controlled by a pixel clock and horizontal and vertical synchronization (sync) signals. Pixels are clocked out of the Swan-2™ ES4318 by the pixel clock. The sync signals determine when the active video data is transferred. The timing of the active video and sync signals is determined by the CRT controller inside the ES4318. The output CRTC timing can be internally generated, or slaved to some other video sync source.

Video Post-Processing

The Swan-2™ ES4318 contains circuitry to post-process video. This circuitry provides color conversion, scaling, and filtering functions through a combination of special hardware and software.

Horizontal up-sampling and filtering is done with a programmable, 7-tap polyphase filter bank for accurate non-integer interpolations. Vertical scaling is achieved by repeating/dropping lines in accordance with the scaling ratio.

Figure 4 shows the video post-processing functional blocks. The first two processing steps are performed by the video processor core. Video post-processing can be applied on the decoded images to improve the picture quality.

The next stage in the processing, applicable only to low resolution MPEG-1 video, is an interlacing filter that generates even and odd fields from decoded frames for applications that use a TV screen. This filter improves both the spatial and temporal appearance of the decoded images on interlaced displays. Following the interlacing filter is an interpolation section that uses bilinear interpolation to increase the resolution of the chrominance components by a factor of two in the vertical dimension.

This interpolation section converts from the MPEG chrominance subsampling to that used by CCIR601. The resulting YUV pixels can then be passed through a 7-tap horizontal interpolation filter that increases the horizontal resolution of the image by up to four times.

The horizontal filter automatically chooses between five sets of filter coefficients based on the fractional component of the new position of the pixel in the video data stream. The filter coefficients are 8 bits wide. The filter length is selectable as 1, 3, 5, or 7 taps.

The relationship between PCLK2XSCN and internal RISC clock is shown in the following table.

Taps	Restrictions	Frequency
3	Pixel rate < (Internal RISC CLK)/2	27 MHz
5	Pixel rate < (Internal RISC CLK)/3	20 MHz
7	Pixel rate < (Internal RISC CLK)/4	default 13.5 MHz

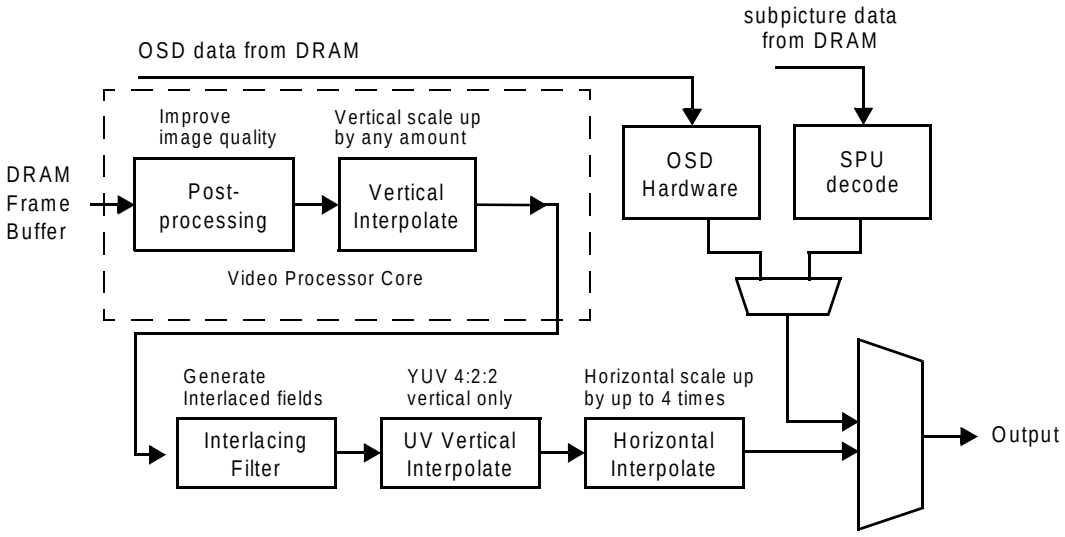


Figure 4 Video Post-processing

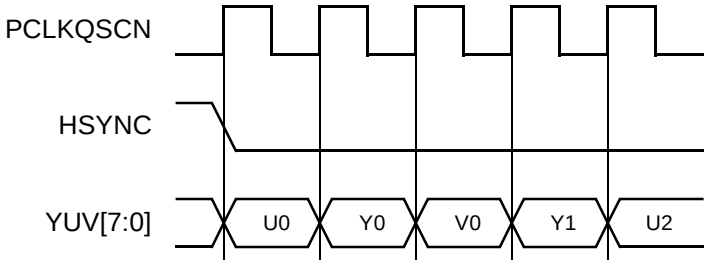


Figure 5 8-bit YUV Input Timing

Video Timing

The video bus can be clocked either by double pixel clock and clock qualifier or by a single pixel clock. The double clock typically is used for TV displays, the single for computer displays. PCLK2XSCN is ignored in 1x clock mode.

The timing of the syncs and odd/even field indication is shown in Figure 6 and Figure 7. The output video field indication is done by modifying the relative positions of VSYNC and HSYNC. At the start of an even field, the horizontal and vertical sync pulses will start on the same clock edge; in odd fields the horizontal sync pulse will be delayed by one clock cycle. The polarity of both horizontal and vertical syncs is programmable.

See the section on Table 4, “Operating AC Characteristics,” on page 18 for a detailed AC timing of the output bus.

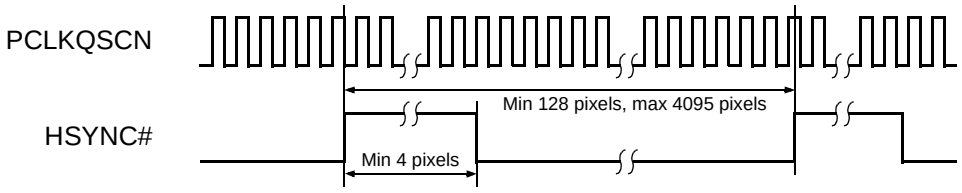


Figure 6 Horizontal Video Timing

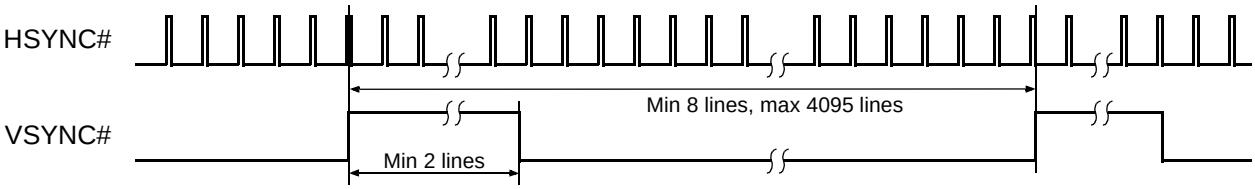


Figure 7 Vertical Video Timing

Sub-Picture Unit

The Sub-Picture unit decodes the run-length Sub-Picture pixel data stream and the corresponding Sub-Picture commands that change the color and contrast values of each pixel type for different regions. The output YUV of the Sub-Picture is blended with the main video screen YUV values, depending on the contrast values.

The Sub-Picture supports four pixel types, coded 00, 01, 10, and 11. Each type represents a color (YUV) and contrast value (blending value with main picture). The Sub-Picture region can also be divided into several horizontal stripes, each potentially with a different set of color/contrast values. Each stripe can be divided vertically into a maximum of 9 vertical regions (default 0, and changes 1-8), each region containing its own color/contrast value for each pixel type. In addition, there is a highlight feature that overrides all other color/contrast information for the Sub-Picture.

Main Sub-Picture commands, such as turning the Sub-Picture unit on/off, setting the Sub-Picture size, default color, and contrast, and the pointers to the color/contrast and pixel data are done by the RISC. The RISC sets the appropriate registers in the Sub-Picture unit, as well as the DMA channel for the command and data FIFOs, based on these commands.

DRAM INTERFACE

The DRAM interface controls access to external DRAM, both SDRAM or EDO, which can be the sole unified external read/write memory acting as program and data memory as well as various decoding and display buffers.

All DRAM control is provided by the Swan-2™ ES4318 DRAM bus. The DRAM interface is 16 bits wide. At high clock speeds, it has sufficient bandwidth to support the decoding and displaying of CCIR601 resolution images at full frame rate.

The ES4318 uses SDRAM with CAS Latency (3) and Sequential Burst of Full Page length. Performance based on SDRAM is double that of EDO. SDRAM must be software configured before any memory access. Frequencies of 100 MHz and 111 MHz are supported (see Table 4 and Table 5). The SDRAM refresh period is programmable to meet any manufacturer's configuration.

If EDO is used the DRAM interface can be programmed to enable support of DRAMs with a variety of page mode cycle times, DRAS to DCAS delay times, and DRAS precharge times. Figure 12 and Figure 13 show the DRAM output signal timing in terms of T states (cycle time) for the Swan-2™ ES4318. The output signals may also be skewed in relation to each other and this should be taken into account when choosing DRAM for any application. The DRAM interface signal skews are shown in Figure 12 and Figure 13.

The Swan-2™ ES4318 DRAM controller uses page mode accesses whenever possible and takes care of DRAM refresh. The ES4318 uses DRAS refresh mode; the refresh period is programmable.

DRAM Configuration Requirements

The DRAM interface generates all the control signals to interface with external DRAM. It supports different configurations using the three configuration bits, sdcfg[2:0], in the BUSCON_DRAM_CONTROL register.

Table 1 shows various memory configuration for both SDRAM and EDO DRAM.

Table 1 Various Memory Configuration

Size in MB	Bit Order sdcfg [2:0]	Memory Configuration
0.5	010	256K x 16-bit (EDO)
1.0	010	2 x 256K x 16-bit (EDO)
2.0	000;001;100;101	1M x 16-bit (SDRAM)
	110	1M x 16-bit (EDO)
2.5	001	1M x 16-bit (SDRAM) + 256K x 16-bit (EDO)
3.0	001	1M x 16-bit (SDRAM) + 2 x 256K x 16-bit (EDO)
4.0	000;100	2 x 1M x 16-bit (SDRAM)
	101	1M x 16-bit (SDRAM) + 1M x 16-bit (SDRAM)
	110	2 x 1M x 16-bit (EDO)
4.5	000	2 x 1M x 16-bit (SDRAM) + 256K x 16-bit (EDO)
5.0	000	2 x 1M x 16-bit (SDRAM) + 2 x 256K x 16-bit (EDO)
6.0	101	1M x 16-bit (SDRAM) + 2 x 1M x 16-bit (EDO)
	100	2 x 1M x 16-bit (SDRAM) + 1M x 16-bit (EDO)
8.0	100	2 x 1M x 16-bit (SDRAM) + 2 x 1M x 16-bit (EDO)

NOTE: It is required that lower memory space (starting 0x 0000 0000) to be mapped to SDRAM if a mix of SDRAM and EDO DRAM is used for the system. Both 16M-bit SDRAM (512K x 16-bit x 2 Bank and the 256 K x 16 or 1M x 16 EDO DRAM in speed of 60 ns are supported.
Refers to bits [13:11] = sdcfg [2:0], see register "BUSCON_DRAM_CONTROL (20008100h, 14-bit, R/W)" on page 52.

DRAM Configuration

Table 2 shows all possible DRAM memory size configuration, each with its corresponding signal pins. DCAS# is always connected. The notation EDO256_0 means the first EDO DRAM 256Kx16, EDO256_1 means the 2nd EDO DRAM 256Kx16, EDO16M_0 means the first EDO DRAM 1Mx16, EDO16M_1 means the 2nd EDO DRAM 1Mx16, SDRAM_0 means the first 16M-bit SDRAM (512Kx2x16), and SDRAM_1 means the 2nd 16M-bit SDRAM.

SDRAM Address Mapping

The memory address (LA) is mapped to the DMA address, which is formed by ADDR in the BUSCON_DMA_ADDR registers. The result is then converted into the DRAM control signals using the SDCF configuration bits in the BUSCON_DMA_CONTROL register.

Table 2 DRAM Memory Size and Signal Pins

Size(MB)	SDRAM 0	SDRAM 1	EDO256_0	EDO256_1	EDO16M_0	EDO16M_1
0.5			DRAS1# DOE#			
1.0			DRAS1# DOE#	DRAS2# DOE#		
2.0					DRAS1# DOE#	
2.0	DRAS0# DCS0#					
2.5	DRAS0# DCS0#		DRAS1# DOE#			
3.0	DRAS0# DCS0#		DRAS1# DOE#	DRAS2# DOE#		
4.0	DRAS0# DCS0#				DRAS1# DOE#	
4.0	DRAS0# DCS0#	DRAS0# DCS1#				
4.5	DRAS0# DCS0#	DRAS0# DCS1#	DRAS1# DOE#			
5.0	DRAS0# DCS0#	DRAS0# DCS1#	DRAS1# DOE#	DRAS2# DOE#		
6.0	DRAS0# DCS0#	DRAS0# DCS1#			DRAS1# DOE#	
8.0	DRAS0# DCS0#	DRAS0# DCS1#			DRAS1# DOE#	DRAS2# DOE#

SDRAM READ AND WRITE TIMING DIAGRAMS

Burst Length = 4, DCAS# Latency

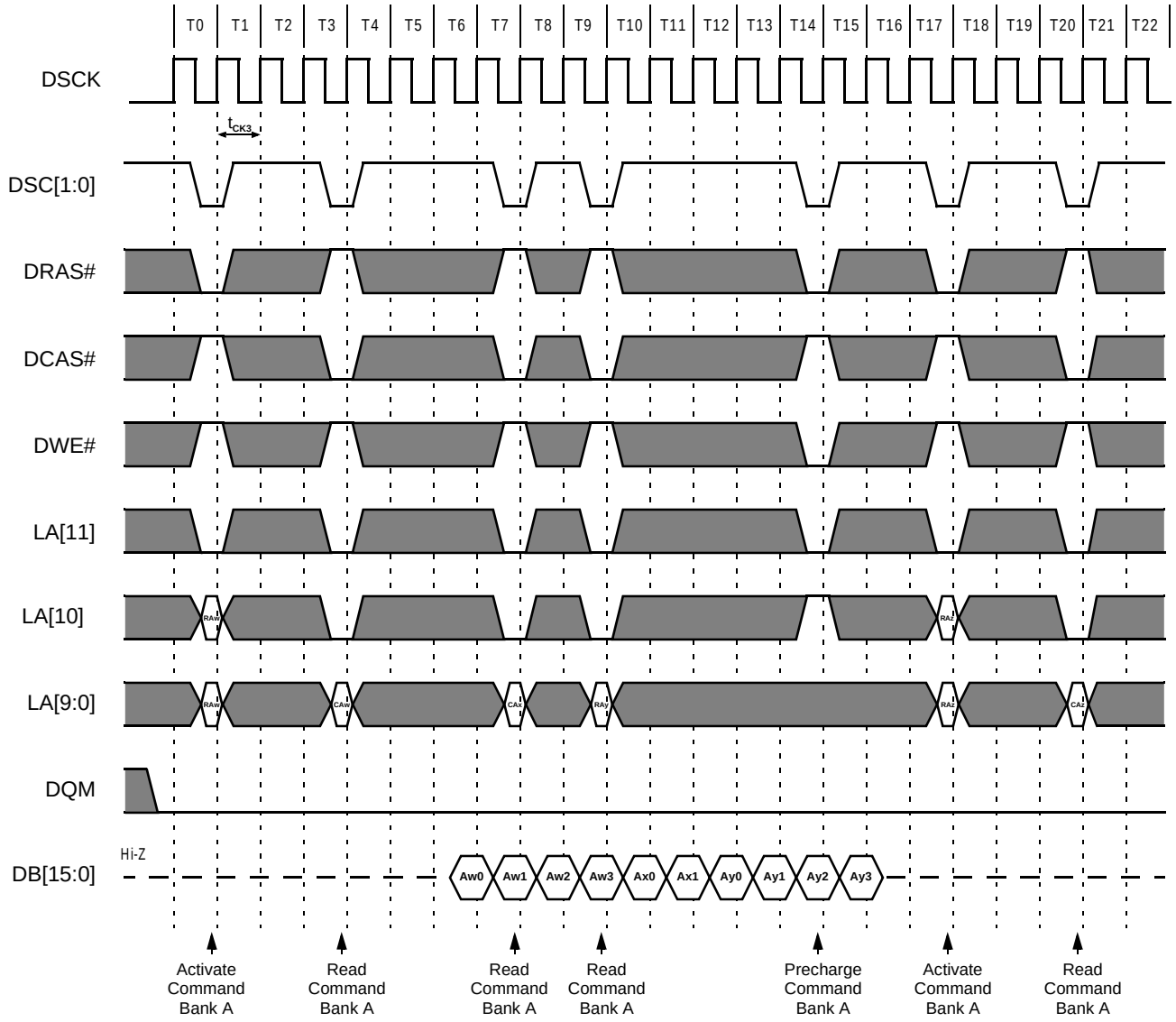


Figure 8 SDRAM Random Column Read Timing

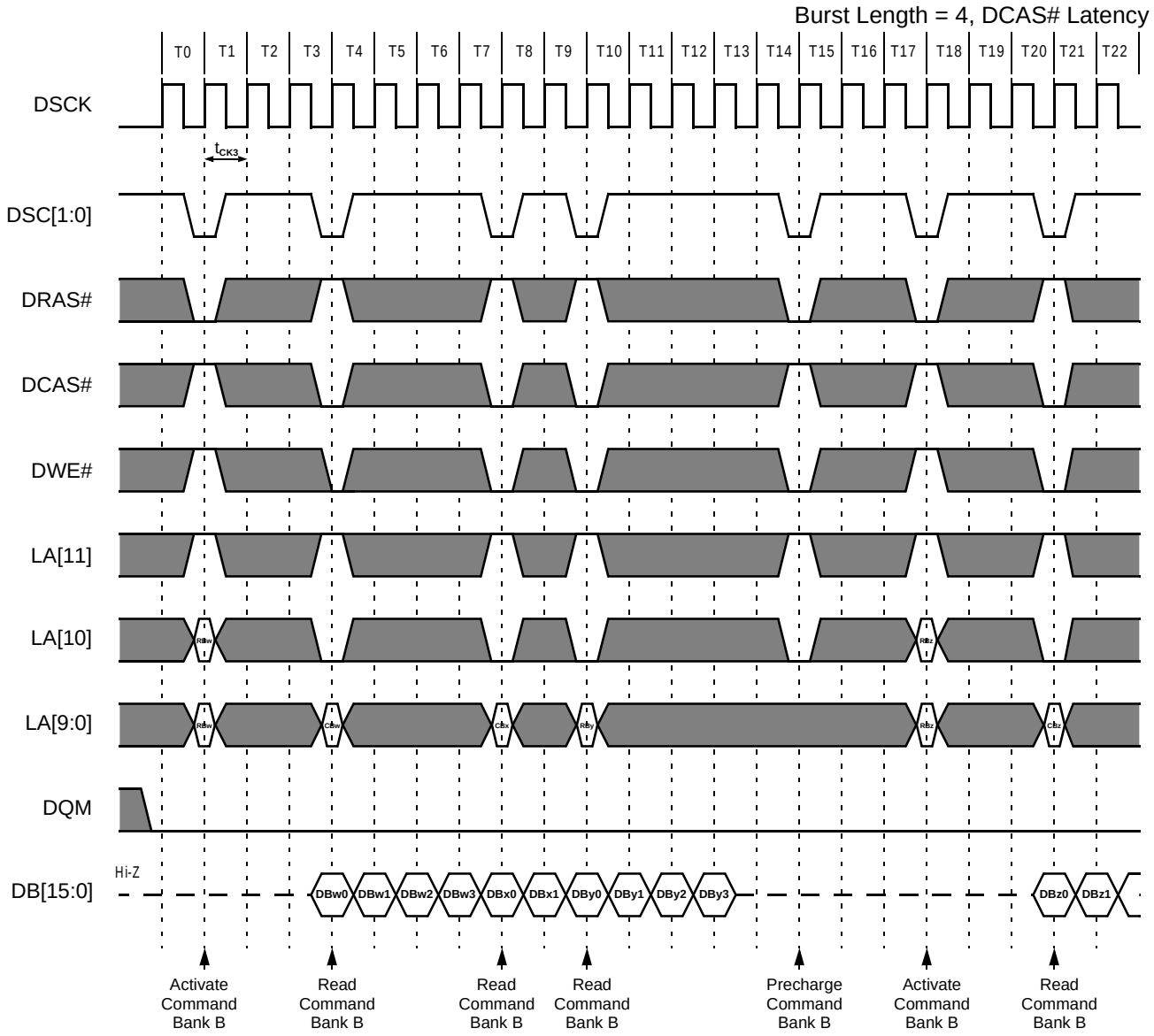


Figure 9 SDRAM Random Column Write Timing

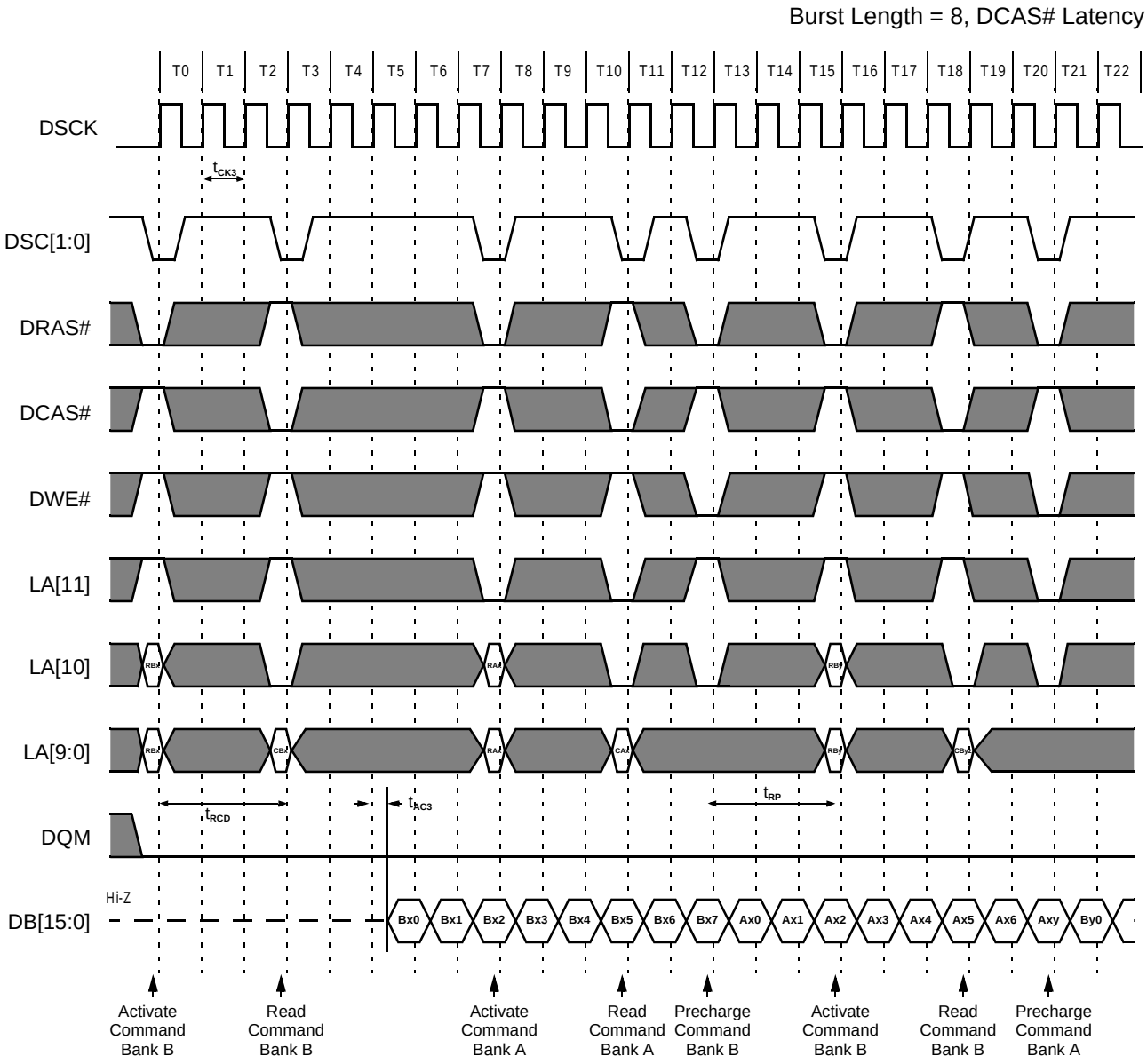


Figure 10 SDRAM Random Row Read Timing

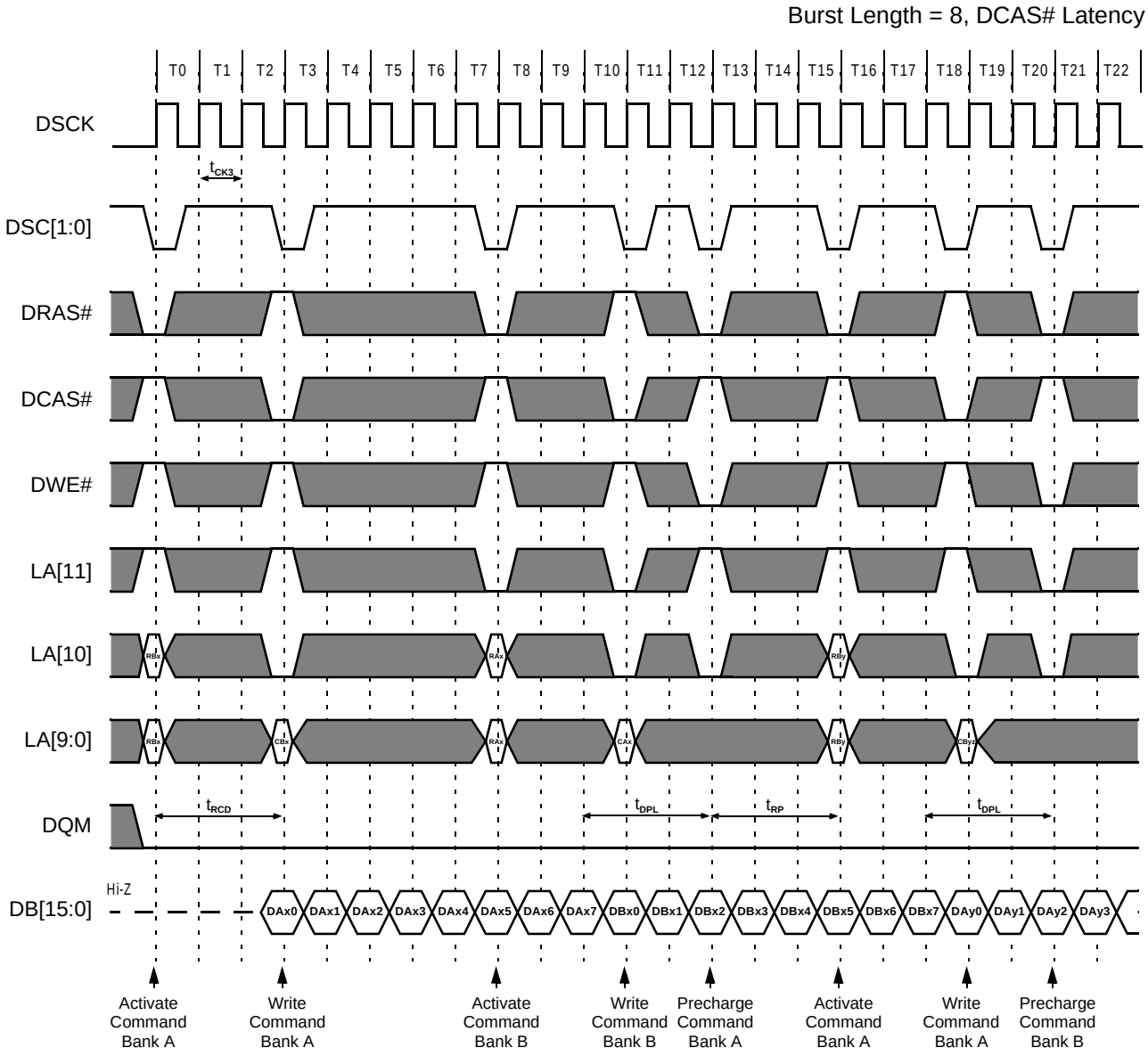


Figure 11 SDRAM Random Row Write Timing

Table 3 SDRAM Interface Timing

Parameter	Symbol	LVTTL		Unit	Note
		-9	-10		
Row active to Row Active Delay	t_{RRD} (min)	18	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ Delay	t_{RCD} (min)	24	26	ns	1
Row precharge time	t_{RP} (min)	24	26	ns	1
Row active time	t_{RAS} (min)	54	60	ns	1
	t_{RAS} (max)	100		µs	
Row cycle time	t_{RC} (min)	90	96	ns	1
Last data in to new column address delay	t_{CDL} (min)	1		CLK	2
Last data in to row precharge	t_{RDL} (min)	1		CLK	2
Last data in to burst stop	t_{BDL} (min)	1		CLK	2
Col. address to column address delay	t_{CCD} (min)	1		CLK	3
Number of valid output data (CAS latency =3)		2		ea	4

Notes:

1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time, and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

Table 4 Operating AC Characteristics

Parameter (CAS Latency = 3)	Symbol	LVTTL				Unit	Note
		-9		-10			
		Min	Max	Min	Max		
CLK cycle time	t_{CC}	9		10		ns	1
CLK to valid output delay	t_{SAC}		7		1.5	ns	1, 2
Output data hold time	t_{OH}	2.5		2.5		ns	2
CLK high pulse width	t_{CH}	3		3.5		ns	3
CLK low pulse width	t_{CL}	3		3.5		ns	3
Input setup time	t_{SS}	2		2.5		ns	3
Input hold time	t_{SH}	0.5		1		ns	3
CLK to output in low-Z	t_{SLZ}	1		1		ns	2
CLK to output in Hi-Z	t_{SHZ}		7		8	ns	

Notes:

1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1 ns, (tr/2-0.5) ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf) = 1ns. If tr & tf is longer than 1 ns, transient time compensation should be considered, that is, [(tr + tf)/2 - 1] ns should be added to the parameter.

Table 5 Frequency vs AC Parameter Relationship (-9)

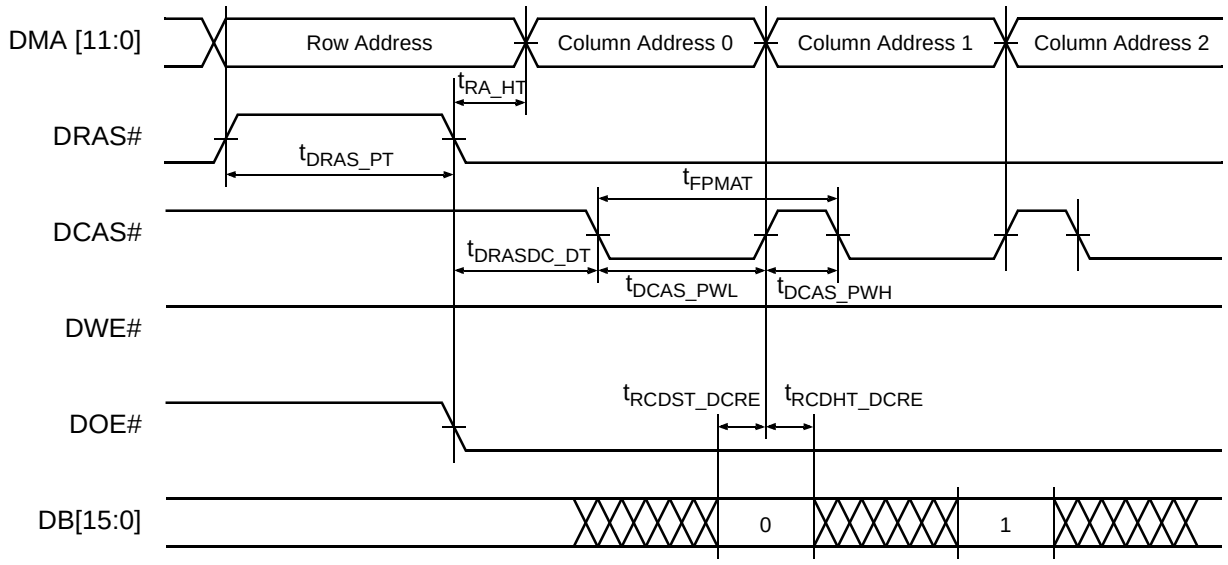
Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{CDL}	t_{RDL}
		90 ns	**54 ns**	**24 ns**	**18 ns**	**24 ns**	**9 ns**	**9 ns**	**9 ns**
111MHz (9.0 ns)	3	10	6	3	2	3	1	1	1

.

Table 6 Frequency vs AC Parameter Relationship (-10)

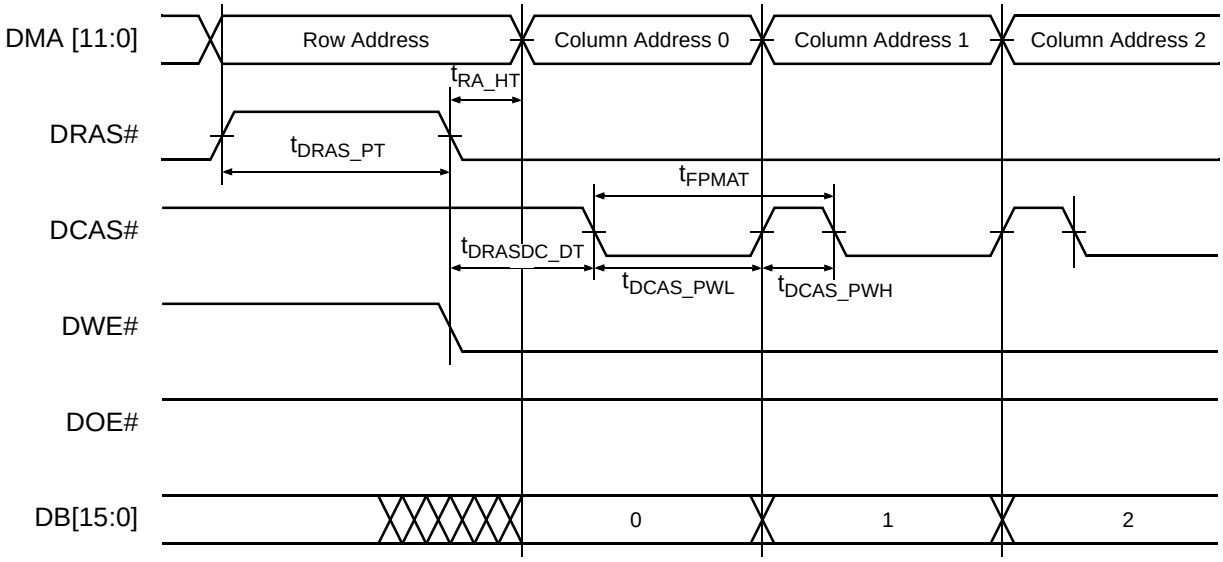
Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{CDL}	t_{RDL}
		96 ns	**60 ns**	**26 ns**	**20 ns**	**26 ns**	**10 ns**	**10 ns**	**10 ns**
100 MHz (10.0 ns)	3	10	6	3	2	3	1	1	1

EDO DRAM READ AND WRITE TIMING DIAGRAMS



Symbol	Parameter	Min	Typ	Max	Units
t_{DRAS_PT}	DRAS precharge time	3		5	internal CPU clock cycle
t_{RA_HT}	Row address hold time	1		3	internal CPU clock cycle
t_{DCAS_PWL}	DCAS pulse width low	1		2	internal CPU clock cycle
t_{DCAS_PWH}	DCAS pulse width high	1		2	internal CPU clock cycle
t_{FPMAT}	Fast page mode access time	2		6	internal CPU clock cycle
t_{DRASDC_DT}	DRAS to DCAS delay time	2		4	internal CPU clock cycle
t_{DRAM_IOSS}	DRAM interface output signal skew	0		3	ns
t_{RCDST_DCRE}	Read cycle data setup time to DCAS rising edge	5		–	ns
t_{RCDHT_DCRE}	Read cycle data hold time to DCAS rising edge	0		–	ns

Figure 12 EDO DRAM Read Timing



Symbol	Parameter	Min	Typ	Max	Units
t_{DRAS_PT}	DRAS precharge time	3		5	internal CPU clock cycle
t_{RA_HT}	Row address hold time	1		3	internal CPU clock cycle
t_{DCAS_PWL}	DCAS pulse width low	1		2	internal CPU clock cycle
t_{DCAS_PWH}	DCAS pulse width high	1		2	internal CPU clock cycle
t_{FPMAT}	Fast page mode access time	2		6	internal CPU clock cycle
t_{DRASDC_DT}	DRAS to DCAS delay time	2		4	internal CPU clock cycle

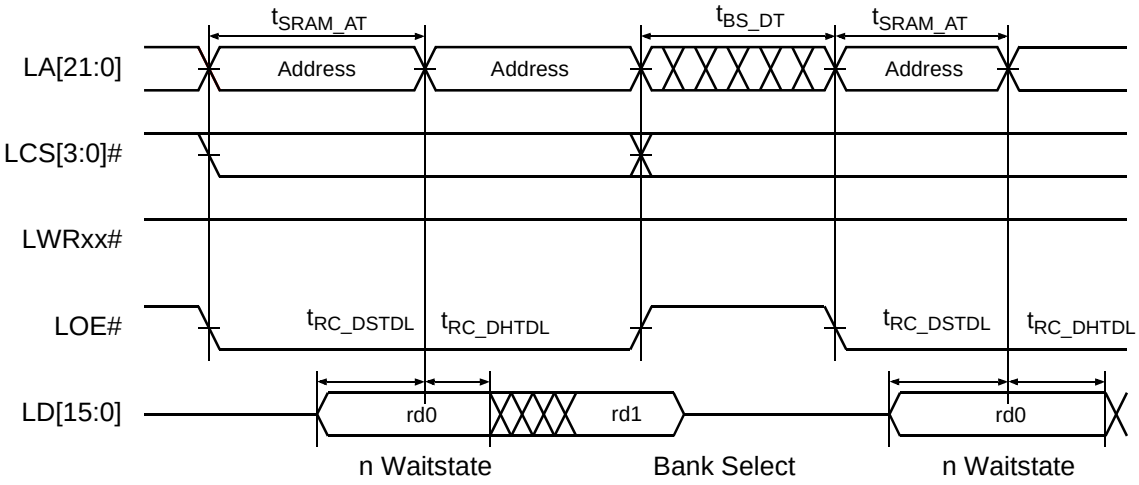
Figure 13 EDO DRAM Write Timing

SRAM INTERFACE

The SRAM interface controls access to optional external SRAM which can be used for RISC code, stack, and data. The SRAM bus supports four independent address spaces, each having programmable bus width and wait states. The interface can support not only SRAM but also ROM/EPROM and memory-mapped I/O ports for standalone applications.

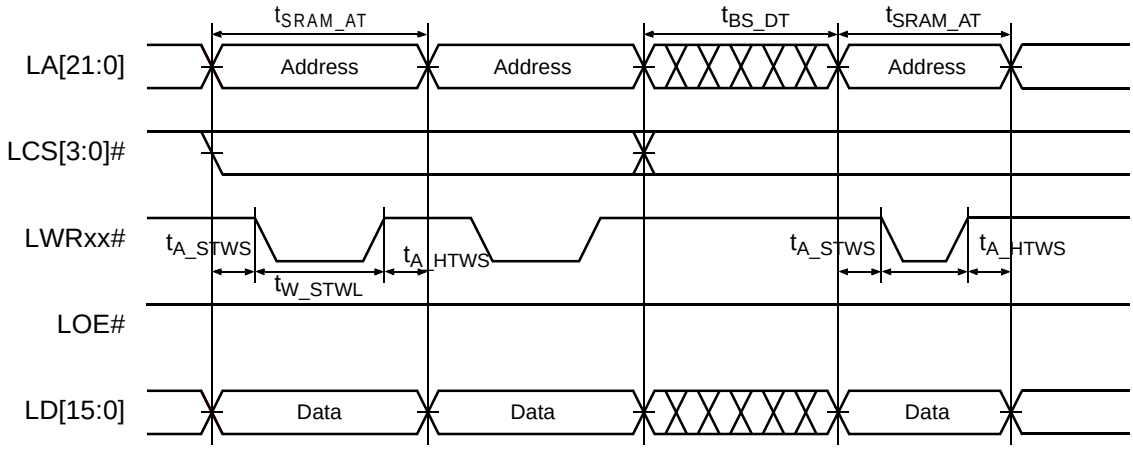
The timing of Swan-2™ ES4318 SRAM access is shown in Figure 14 and Figure 15. From 1 to 32 wait states can be inserted into each cycle, each wait state being one Swan-2™ ES4318 CLOCK cycle long. RISC accesses can involve just one wait state. It is possible, when switching from a low speed bank to a high speed bank, for the turnoff delay of the low speed bank to overlap the first access of the high speed bank. To prevent data corruption, t_{BS_DT} (bank select delay time) is programmable for each bank from 0 to 3T states.

The signals for the SRAM bus are generated from the internal RISC clock and are timed in integer multiples of clock cycles, except for the write strobe, which is delayed by 1/2 cycle from the address setup and advanced 1/2 cycle from the start of the next access cycle. The SRAM interface signal skew may vary with Swan-2™ ES4318 speed grade. See Figure 14 and Figure 15 for details.



Symbol	Parameter	Min	Typ	Max	Units
t_{DRAM_IOSS}	DRAM interface output signal skew	0		3	ns
t_{RC_DSTDL}	Read cycle data setup time to data latch	6		–	ns
t_{RC_DHTDL}	Read cycle data hold time to data latch	2		–	ns
t_{SRAM_AT}	SRAM access time	2*		33	internal CPU clock cycle
t_{BS_DT}	Bank Select delay time	0		3	internal CPU clock cycle

Figure 14 SRAM Read Timing



Symbol	Parameter	Min	Typ	Max	Units
t_{SRAM_IOSS}	SRAM interface output signal skew	0		3	ns
t_{SRAM_AT}	SRAM access time	2*		33	internal CPU clock cycle
t_{BS_DT}	Bank Select delay time	0		3	internal CPU clock cycle
t_{A_STWS}	Address setup time to write strobe	0.5		0.5	internal CPU clock cycle
t_{A_HTWS}	Address hold time to write strobe	0.5		0.5	internal CPU clock cycle
t_{W_STWL}	Write strobe pulse width low	1		31.5	internal CPU clock cycle

Figure 15 SRAM Write Timing

TDM INTERFACE

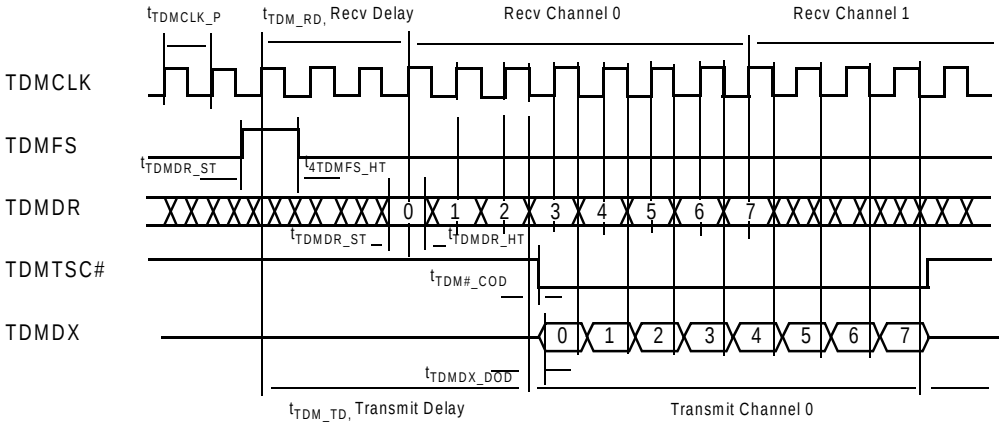
The TDM interface implements a five-wire serial bus which provides an easy connection between the Swan-2™ ES4318 and available communications chips. The TDM Interface is a time division multiplexed bus that multiplexes data on up to 64 channels. Each channel is allocated a different time slot on the bus and the ES4318 can be set to send and receive data in any combination of different time slots. Data is assumed to be ordered by time slot, e.g., if time slots 6, 8, and 17 are used, the first DMA byte sent to memory would be in time slot 6, followed by time slots 8 and 17 in order. Reordering must be done in software.

The interface consists of a Frame Sync (TDMFS), data transmit, and receive signals (TDMDX and TDMDR), external buffer enable (TDMTSC#), and a clock (TDMCLK). The timing of the data transfer is externally controlled.

The TDM interface can support a number of different timings. The timing diagram, Figure 16, is shown for a particular configuration.

The TDM Interface can transfer data at a maximum rate of 16 Mbps. A more typical configuration would support up to 4.096 Mbps with a TDMFS frequency of 8 KHz. The TDM interface hardware is flexible enough to interface with a wide range of communications chips for ISDN, PABX, LAN, and WAN connectivity. In particular, it will interface directly to chips that support the concentration highway interface (CHI), ISDN-oriented modular revision 2 (IOM-2) interface, and multi-vendor integration protocol (MVIP).

The TDM Interface programmability includes independent receive, transmit, and frame sync clock edge selection and independent receive and transmit data offsets. This is illustrated in Figure 16.



Symbol	Parameter	Min	Typ	Max	Units
t_{TDMCLK_P}	TDM clock period	62.5		–	ns
$t_{TDM\#\_COD}$	TDMTSC# control output delay to TDM-CLK	0		2	
t_{TDMFS_ST}	TDMFS setup time to TDMCLK	4		–	
t_{4TDMFS_HT}	TDMFS hold time to TDMCLK	2		–	
t_{TDMDR_ST}	TDMDR data setup time to TDMCLK	4		–	
t_{TDMDR_HT}	TDMDR data hold time to TDMCLK	2		–	
t_{TDMDX_DOD}	TDMDX data output delay to TDMCLK	0		2	
t_{TDM_RD}	TDM receive delay to TDMFS	0		8	internal CPU clock cycle
t_{TDM_TD}	TDM transmit delay to TDMFS	0		8	internal CPU clock cycle

Figure 16 TDM Interface Timing

HOST INTERFACE

The host interface is used by an external host to control the Swan-2™ ES4318 and may also be used to transfer high or low speed user data, audio, and bitstream information. The host interface is a generic 16-bit parallel bus that accesses six registers in the ES4318. The registers and their functions are detailed in the register description section. Figure 17 shows the timing for the host interface.

There are three ports in the host interface, a debug port, a command port, and a DMA port.

The host interface is implemented with a 16-bit data bus, a 3-bit address bus, read and write strobes, and request lines. The request lines indicate when data is waiting for the host to read or write data. The lines can be programmed for any combination of the DMA, command, or debug ports.

Debug Port

The debug port provides a path to the Swan-2™ ES4318 RISC processor to allow software debuggers access to the hardware and software state without disturbing the command or DMA ports.

Command Port

The Command port transfers commands and status information between the Swan-2™ ES4318 and an external host. In some systems, the ES4318 acts as the system controller, so there is no external host.

In computer-based systems where a microprocessor is responsible for controlling the system, it controls the Swan-2™ ES4318 through the command port using that port's “shared variable” mechanism. This gives the host read/write access to global control variables in the ES4318 and provides a simple and effective control mechanism.

DMA Port

The DMA port is typically used for transferring user data (graphics, program executables, etc.). For some applications, the audio, video, or system multiplexed bitstreams can be carried over this interface.

The host interface on the Swan-2™ ES4318 uses the HRDREQ# and HWRREQ# pins to indicate it is ready to send and receive data. The HIRQ pin is used to indicate that the H_HOSTIRQSTAT register should be interrogated.

DCI INTERFACE

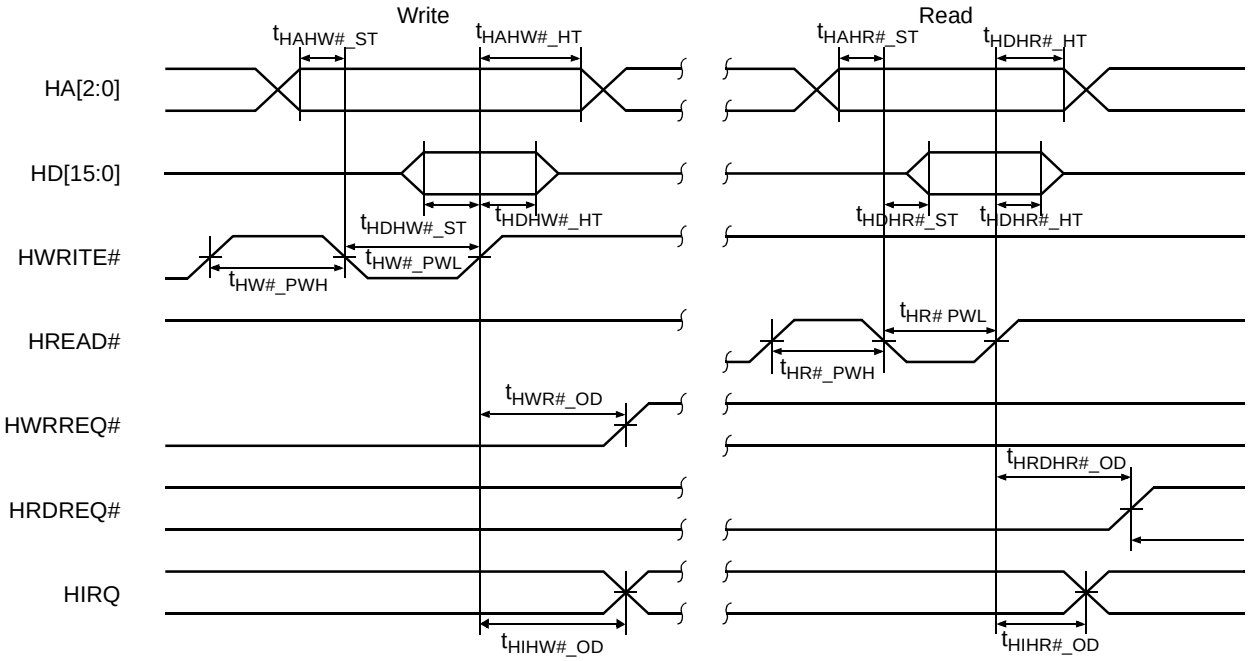
In addition to TDM (serial interface) and Host (parallel interface), the Swan-2™ ES4318 offers DCI, a direct interface to the DVD loader. This 8-bit parallel interface meets the specification of many DVD loader manufacturers.

Figure 18 shows the DCI interface timing. DCI_FDS# indicates the beginning of each sector. The DCI_ERR# signal indicates the error per data byte. DCI_ACK# indicates an acknowledge signal from the servo that a data byte is ready to be transferred. The DCI_REQ# line indicates that the ES4318 has to inform the servo that it is ready to receive data.

AUDIO INTERFACE

The Swan-2™ ES4318 audio port is limited to support of 2 channel stereo audio in I²S format. Its configuration is software selectable and interfaces directly with low-cost audio DACs and ADCs. In this mode, the audio input clock should be 256Fs, 384Fs, and 512Fs, where Fs is usually 32 KHz, 44.1 KHz, 48 KHz, or 96 KHz.

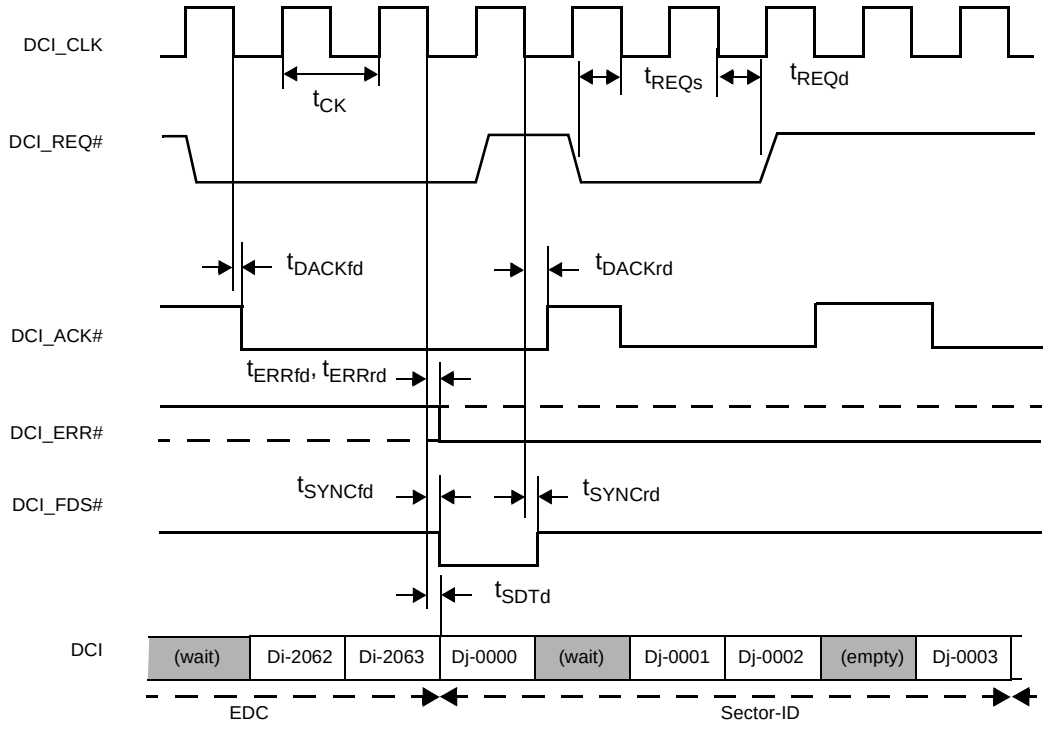
MCLK is the audio DAC clock and can either be an output from or an input to the Swan-2™ ES4318. Audio data in is handled symmetrically to the audio data out phase.The audio data out (TSD), audio transmit frame sync (TWS), and audio receive frame sync (RWS) are driven by the audio transmit bit clock (TBCK). The audio data out (TSD) is driven by the audio receive bit clock (RBCK).



Symbol	Parameter	Min	Typ	Max	Units
$t_{HAHW\#\_ST}$	HA to HWRITE# setup time	4		–	
$t_{HAHW\#\_HT}$	HA to HWRITE# hold time	2		–	
$t_{HDHW\#\_ST}$	HD to HWRITE# setup time	4		–	
$t_{HDHW\#\_HT}$	HD to HWRITE# hold time	2		–	
$t_{HW\#\_PWL}$	HWRITE# pulse width low	30		–	
$t_{HW\#\_PWH}$	HWRITE# pulse width high	30		–	
$t_{HWR\#\_OD}$	HWRREQ# to HWRITE# output delay	0		8	
$t_{HAHR\#\_ST}$	HA to HREAD# setup time	4		–	
$t_{HAHR\#\_HT}$	HA to HREAD# hold time	2		–	
$t_{HDHR\#\_ST}$	HD to HREAD# setup time	0		4	
$t_{HDHR\#\_HT}$	HD to HREAD# hold time	2		–	
$t_{HR\#\_PWH}$	HREAD# pulse width high	30		–	
$t_{HR\#\ PWL}$	HREAD# pulse width low	30		–	
$t_{HRDHR\#\_OD}$	HRDREQ# to HREAD# output delay	0		8	
$t_{HIHW\#\_OD}$	HIRQ to HWRITE# output delay	0		8	
$t_{HIHR\#\_OD}$	HIRQ to HREAD# output delay	0		8	

Figure 17 Host Bus Timing

DCI Timing



Symbol	Parameter	Min	Typ	Max	Units
t_{CK}	CSTROBE output frequency		3.375		MHz
t_{REQs}	REQUEST setup time	100			ns
t_{REQh}	REQUEST hold time	0			ns
t_{DACKrd}	DACK rising edge delay	0		5	ns
t_{DACKfd}	DACK falling edge delay	0		5	ns
t_{ERRrd}	ERROR rising edge delay	0		5	ns
t_{ERRfd}	ERROR falling edge delay	0		5	ns
t_{SYNCrd}	SYNC rising edge delay	0		5	ns
t_{SYNCfd}	SYNC falling edge delay	0		5	ns
t_{SDTd}	SDT[7:0] delay time	0		5	ns

Figure 18 DCI Interface Timing

Audio Transmit and Receive Timing Diagrams

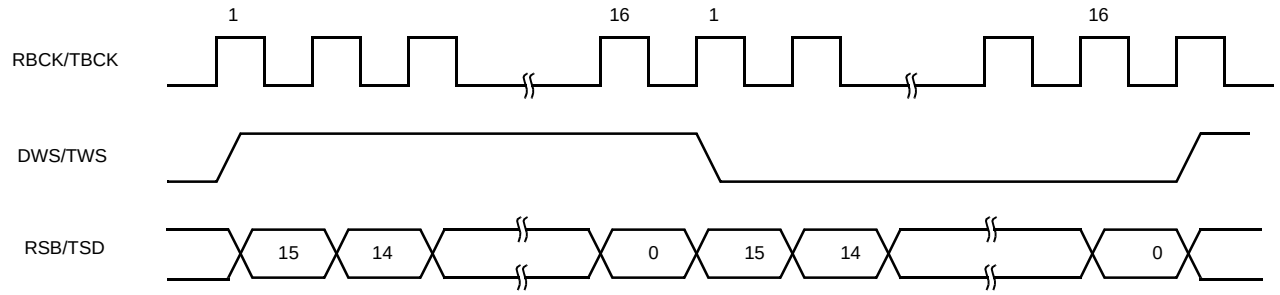


Figure 19 Right Justified Mode / 16-Bit Cycle Frame / 16-Bit Data Frame

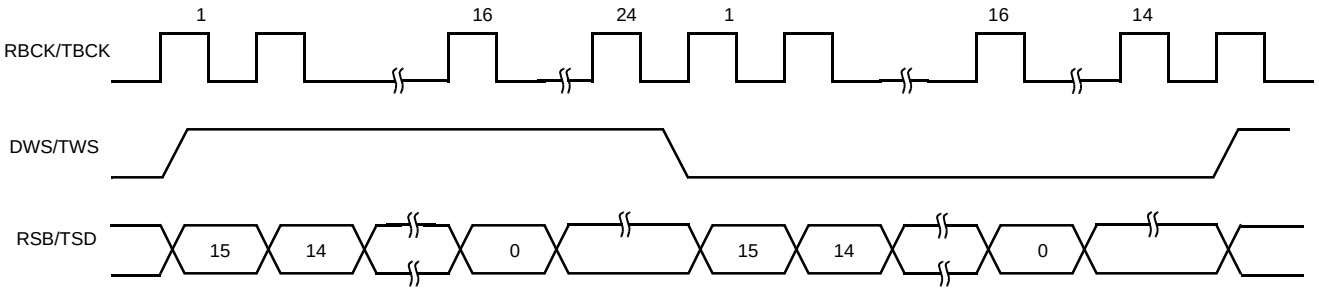


Figure 20 Right Justified Mode / 24-Bit Data Frame / First-Bit Sent First / MSB First

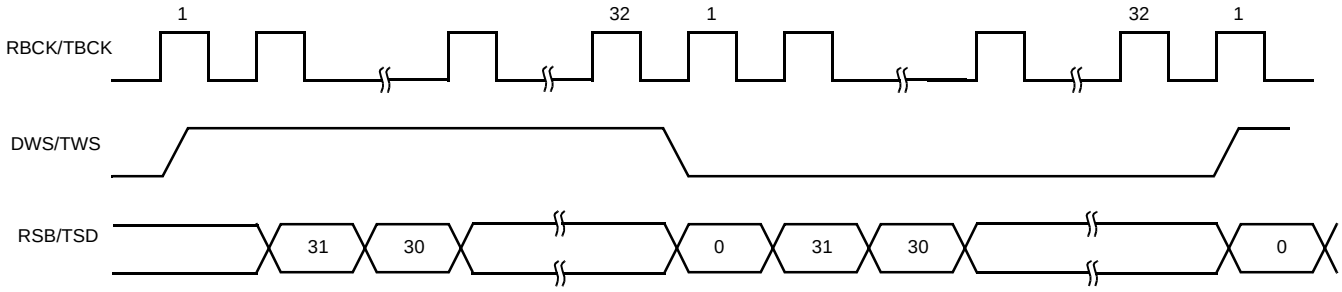


Figure 21 Right Justified Mode / 32-Bit Cycle Frame / 24-Bit Data Frame / Last Bit Sent Last / LSB First

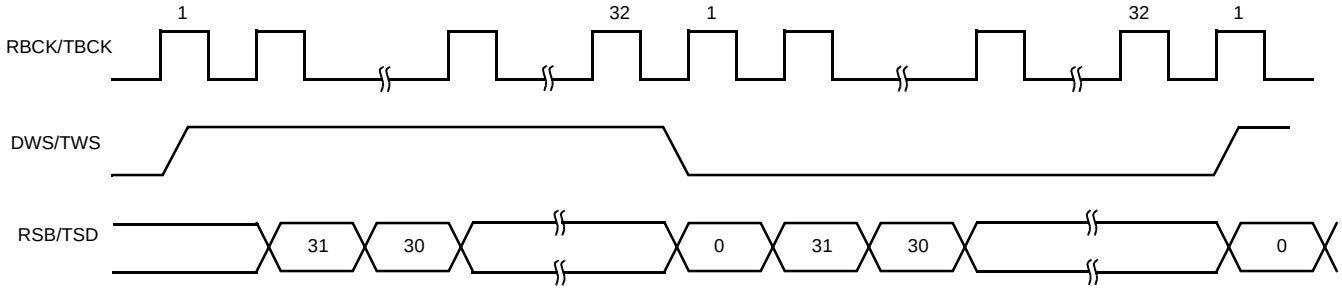


Figure 22 Left Justified Mode / 32-Bit Cycle Frame / 32-Bit Data Frame / MSB Firs

REGISTERS

TDM Registers

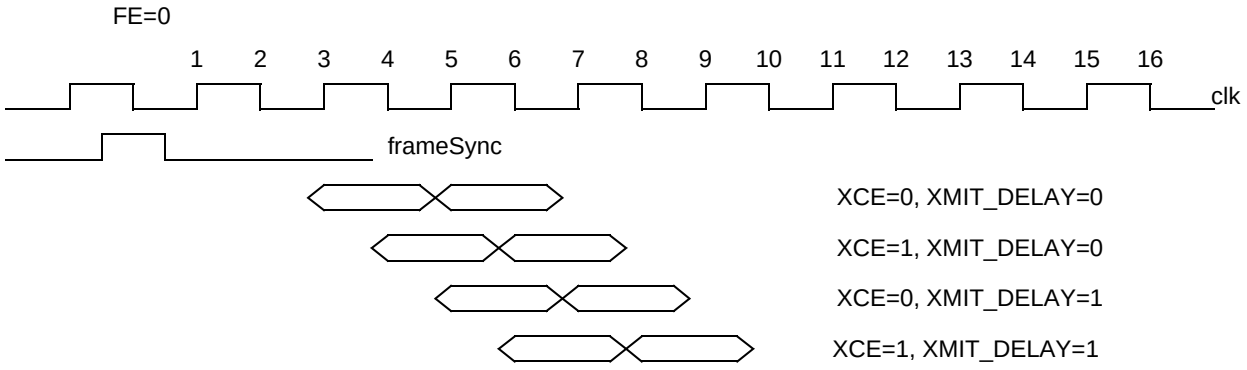
The TDM registers allows the RISC processor to receive and transmit data from the serial Time Division Multiplex (TDM) interface.

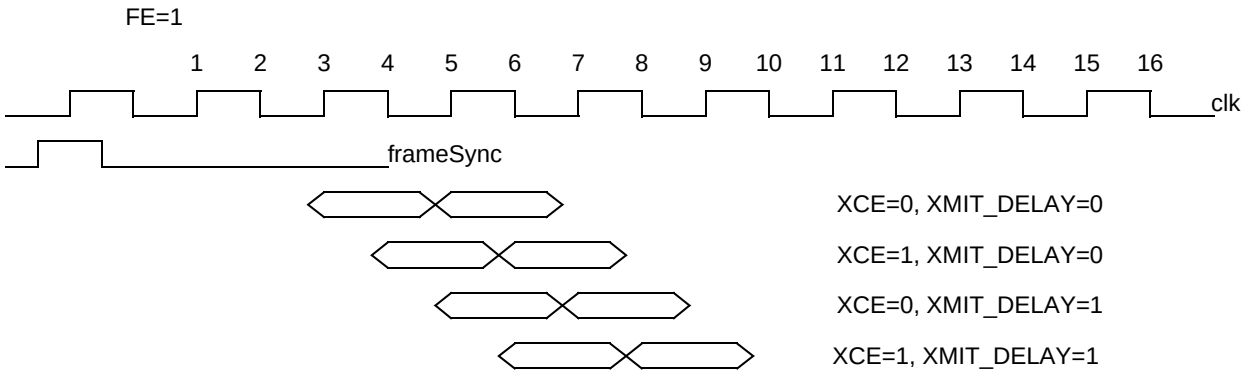
TDM Operation and Bit Settings:

1. To turn on the TDM, set the tdm_rst bit (bit 5) in the TDMCTL0 register to 0, then to 1.
2. To reset the TDM internal registers, set tdm_tstbit (bit 10) in the TDMCTL0 register to 1, then to 0.
3. The slot registers must be set, there are no default values.
4. When using 2x clock, the crefphase bit has to be set and the p bit in the XMT/RCVDELAY register must be 0.
5. When using 2x clock, the values in tables must be multiplied by 2.

6. FE, XCE, XMT_DELAY table:

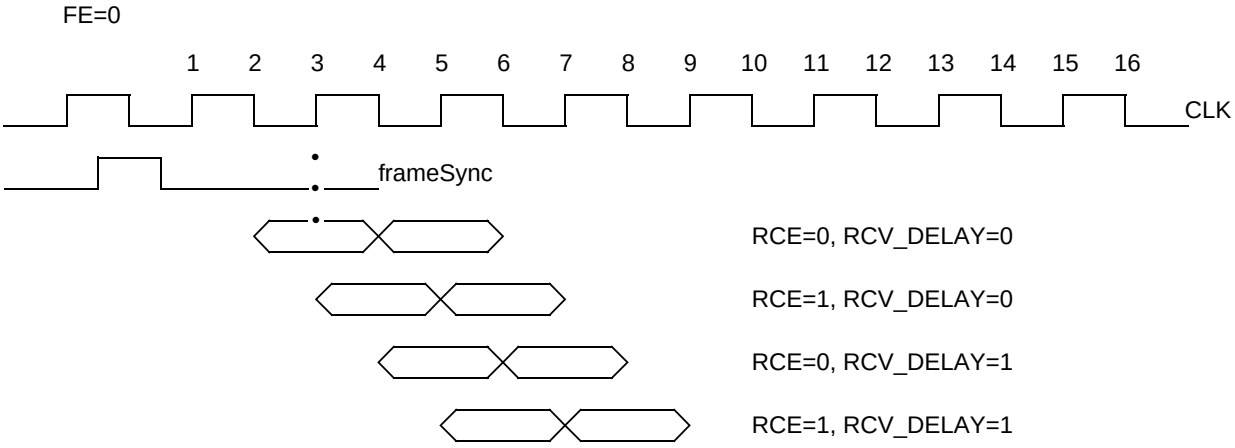
		XMT_DELAY								
FE	XCE	0	1	2	3	4	5	6	7	Note
0	0	3	5	7	9	11	13	15	17	start x-mit on rising
0	1	4	6	8	10	12	14	16	18	start x-mit on falling
1	0	3	5	7	9	11	13	15	17	start x-mit on falling
1	1	4	6	8	10	12	14	16	18	start x-mit on rising

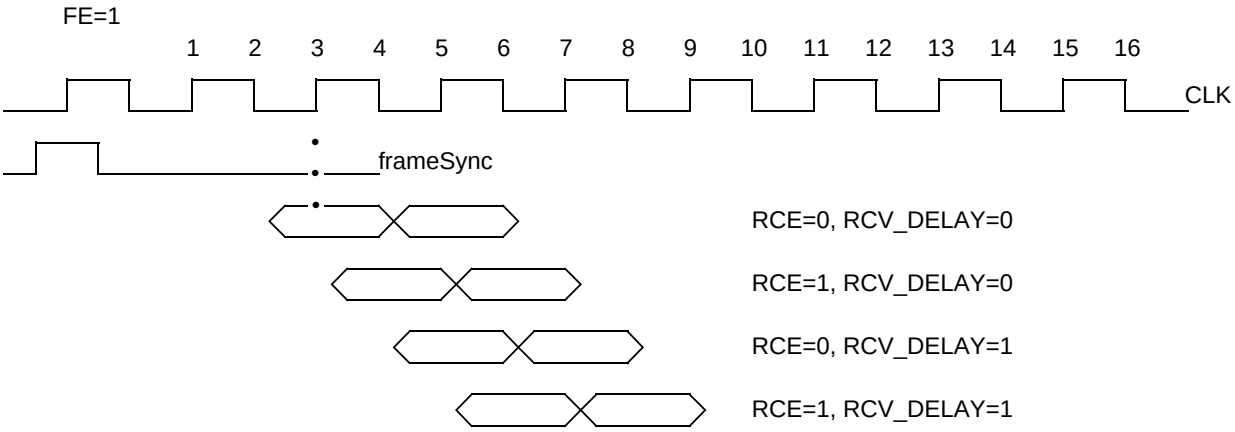




7. FE, XCE, RCV_DELAY table:

		RCV_DELAY								
FE	RCE	0	1	2	3	4	5	6	7	Note
0	0	4	6	8	10	12	14	16	18	sampled on falling
?	1	3	5	7	9	11	13	15	17	sampled on rising
?	0	4	6	8	10	12	14	16	18	sampled on rising
?	1	3	5	7	9	11	13	15	17	sampled on falling





TDMXMTDELAY (2000E004h, 4-bit, R/W)

x				delay			p
7	6	5	4	3	2	1	0

This register allows a variable delay from the start of frame sync to the start of valid data (for data transmitted from RISC to TDM).

Bits	Name	Description
7:4	–	Reserved.
3:1	delay	Delay value in milliseconds.
0	p	Phase delay. For normal operation set to 1 (test bit).

TDMRCVDELAY (2000E008h, 4-bit, R/W)

x				delay			p
7	6	5	4	3	2	1	0

This register allows a variable delay from the start of frame sync to the start of valid data (for data transmitted from TDM to RISC).

Bits	Name	Description
7:4	–	Reserved.
3:1	delay	Delay value in milliseconds.
0	p	Phase delay. For normal operation set to 1 (test bit).

TDMCTL0 (2000E00Ch, 16-bit, R/W)

tdm interface control bits							
15	14	13	12	11	10	9	8
tdm interface control bits							
7	6	5	4	3	2	1	0

This register contains the control bits for the TDM Interface. After reset, it is initialized to 0x0000.

Bits	Name	Description
15	tdm2xpt	0 = Allow data transfer from TDM to RISC. 1 = Allow data transfer from TDM to xport.
14	rstflowbits	1 = Reset the underflow and overflow flags.
13	oflowmask	0 = Otherwise. IRQ mask for the receive overflow flag (for code development).
12	uflwmask	IRQ mask for the transmit underflow flag (for code development).
11	testrdslot	1 = Read the values in the tdmslots (controls mux).
10	testrst	Resets the internal registers for testing: 1 = Reset.
9	xmtendian	Controls big endian or little endian select: 0 = Big endian. 1 = Little endian.
8	rcvendian	Controls big endian or little endian select: 0 = Big endian. 1 = Little endian.
7	crefphase	Controls the phase of the cref2x signal when using a 2x serial clock.
6	fe	Selects the edge of the input serial clock to use (see below).
5	rst	Software reset for the TDM: 0 = Reset.
4	tre_msk	IRQ mask for interrupt to the RiscMVD: 1 = IRQ enabled. 0 = IRQ off.
3	dw_msk	Irq mask for interrupt to the RiscMVD: 1 = IRQ enabled. 0 = IRQ off.
2	rce	The clock edge to use for receiving (see below).
1	xce	The clock edge to use for transmitting (see below).
0	sel2x	1 = Input clock is 2x the pixel rate.

TDMCTL1 (2000E01Ch, 8-bit, R/W)

auto_fen	xaform	semsk	clrselrq	gw2tdm	edcen	dscren	xamode
7	6	5	4	3	2	1	0

This register contains control bits for the TDM Interface. After reset, it is initialized to 0x00.

Bits	Name	Description
7	auto_fen	Auto-form detect enable.
6	xaform	When the auto_fen is disabled, firmware to inform the hardware about the form of entry data: 0 = xa mode 2 form 1 (default). 1 = xa mode 2 form 2.
5	semsk	Mask the sector end interrupt to RISC.
4	clrseirq	Writing a 1 to this bit clears the sector end interrupt from TDM to RISC. This interrupt is generated at the end of each sector, so the RISC can read the TDMSTATUS1 register for status of the previous sector.
3	gw2tdm	0 = Allow data transfer from RISC to TDM. 1 = Allow data transfer from gateway to TDM.
2	edcen	Enable fast edc.
1	dscren	Enable the discrambler.
0	xamode	0 = Yellow book. 1 = XA mode 2.

TDMXMTSLOTS (2000E020h–2000E03Ch, 8-bit, R/W)

d							
7	6	5	4	3	2	1	0

The table below gives the time slot values for the transmitter. To read these registers, set testrdslots in the TDMCTL register. This disables the operation of the TDM, so use only for testing.

Hexadecimal Address	Bit Position							
	0	1	2	3	4	5	6	7
2000E020h	0	1	2	3	4	5	6	7
2000E024h	8	9	10	11	12	13	14	15
2000E028h	16	17	18	19	20	21	22	23
2000E02Ch	24	25	26	27	28	29	30	31
2000E030h	32	33	34	35	36	37	38	39
2000E034h	40	41	42	42	44	45	46	47
2000E038h	48	49	50	51	52	53	54	55
2000E03Ch	56	57	58	59	60	61	62	63

TDMRCVSLOTS (2000E040h–2000E05Ch, 8-bit, W/R)

d							
7	6	5	4	3	2	1	0

The table below gives the time slot selection for the receiver. To read these registers, set testrdslots in the TDMCTL register. This disables the operation of the TDM, so use only for testing.

Hexadecimal Address	Bit Position							
	0	1	2	3	4	5	6	7
2000E040h	0	1	2	3	4	5	6	7
2000E044h	8	9	10	11	12	13	14	15
2000E048h	16	17	18	19	20	21	22	23
2000E04Ch	24	25	26	27	28	29	30	31
2000E050h	32	33	34	35	36	37	38	39
2000E054h	40	41	42	42	44	45	46	47
2000E058h	48	49	50	51	52	53	54	55
2000E05Ch	56	57	58	59	60	61	62	63

Host Interface (RISC side) Registers

The following describes the host interface RISC side registers.

R_HOSTDMAPORT (0x20003000 16-bit R/W)

d							
15	14	13	12	11	10	9	8
d							
7	6	5	4	3	2	1	0

This register contains data transferred to/from the host (DMA port). After reset, it is initialized to 0x0000.

R_HOSTVCXPORT (0x20003004 8-bit R/W)

d							
7	6	5	4	3	2	1	0

This register contains data transferred to/from the host (VCX port). After reset, it is initialized to 0x00.

R_HOSTDBGPORT (0x20003008 8-bit R/W)

d							
7	6	5	4	3	2	1	0

This register contains data transferred to/from the host (debug port). After reset, it is initialized to 0x00.

R_HOSTMASK (20003010h, 8-bit, R/W)

endn sel	dbg dw	dbg tre	dma dw	dma tre	vcxi dw	vcxi tre	h2r irq
7	6	5	4	3	2	1	0

This register contains the mask bits for interrupts from the host to the RISC. After reset, it is initialized to 0.

Bits	Name	Description
7	endnsel	Endian select; 1 = switch upper/lower bytes when write R_HOSTDMAPORT.
6:0		Mask bits for interrupts from the host to the RISC.

R_HOSTIRQSTAT (20003014h, 8-bit, R)

x						dcierr	dciirq
15	14	13	12	11	10	9	8
r2hirq	dbg tre	dbg dw	dma tre	dma dw	vcxi tre	vcxi dw	h2irq
7	6	5	4	3	2	1	0

This register reads the status of Interrupts from the host to the RISC; 1=IRQ, 0=no IRQ.

Bits	Name	Description
9	dcierr	1 = previous sector has error.
8	dciirq	Sector-end interrupt from DCI port to RISC.
7	r2hirq	Interrupt flsg set by the RISC as a signal to the host.
6	dbgtre	Debug transmit register empty (OK for RISC to send data to the host).
5	dbgdw	Debug data waiting (RISC needs to read data from the host).
4	dmatre	DMA transmit register empty (OK for RISC to send data to the host).
3	dmadw	DMA data waiting (RISC needs to read data from the host).
2	vcxitre	VCXI transmit register empty (OK for RISC to send data to the host).
1	vcxidw	VCXI data waiting (RISC needs to read data from the host).
0	h2irq	Interrupt flag set by the host as a signal to the RISC.

R_IDEDAT (0x20003018 16-bit R/W)

d							
15	14	13	12	11	10	9	8
d							
7	6	5	4	3	2	1	0

This register contains data sent/received to/from ATAPI slave, in master mode. After reset, it is initialized to 0x0000.

R_IDEADDR (0x2000301C 3-bit R/W)

x					a		
7	6	5	4	3	2	1	0

This register contains address sent to ATAPI slave, in master mode. After reset, it is initialized to 0x0.

R_IDECTL (0x20003020 13-bit R/W)

x			clr iirq	ide2 xpt	ide st	ide rst	ide msk 1
15	14	13	12	11	10	9	8
ide msk 0	ide cs	hst mode	ide en	ide rw	mode 2	mode 1	mode 0
7	6	5	4	3	2	1	0

After reset, it is initialized to 0x0000.

Bits	Name	Description
15:8	–	Reserved.
12	clriirq	Write 1 to clear sector-end interrupt from ATAPI slave.
11	ide2xpt	In master mode, write 1 to this bit to enable data transfer from ATAPI data port to RISC. Data transfer will continue on until this bit is reset to 0.
10	idest	write 1 to signal the beginning of the sector. The sector start signal will be reset by the first data valid.
9	iderst	Write 1 to reset the ATAPI slave, then write 0 to unreset. The ATAPI slave will also be reset at the same time with the ES4318.ides.
8	idemsk1	Mask sector-end interrupt from ATAPI to RISC.
7	idemsk0	Mask interrupt from ATAPI to RISC.
6	idecs	0 = assert cs1fx. 1 = assert cs3fxb.
5	hstmode	0 = slave mode. Host will receive commands or data from DVD-DSP. 1 = master mode. Host will send read/write commands (comply to ATAPI) idec.
4	ideen	Enable the host to write/read to/from the ATAPI slave.
3	iderw	1 = read from ATAPI slave. 0 = write to ATAPI slave.
0:2		ATAPI modes 0-4.

R_IDESSTAT (0x20003024 3-bit W)

x					ide irq	ide 16	ide val
7	6	5	4	3	2	1	0

Bits	Name	Description
7:3	-	Reserved.
2	ideirq	1 = Sector-end interrupt from ATAPI slave to RISC.
1	ide16	Read only bit 1 = 16-bit transfer. If reading from ATAPI slave, all 16-bit data of R_IDEDAT are valid. If writing to ATAPI slave, all 16-bit data of R_IDEDAT are received at the ATAPI slave. 0 = 8-bit transfer. If reading from ATAPI slave, only the last 8-bits of R_IDEDAT are valid. If writing to ATAPI slave, only the last 8-bits of R_IDEDAT are received at the ATAPI slave.
0	ideval	1 = pio cycle is completed. In read mode, read from R_IDEDAT to retrieve the data from the ATAPI slave; write 1 to clear this bit.

R_IDECNT (0x20003028 12-bit R/W)

x				ide cnt 11	ide cnt 10	ide cnt 9	ide cnt 8
15	14	13	12	11	10	9	8
ide cnt 7	ide cnt 6	ide cnt 5	ide cnt 4	ide cnt 3	ide cnt 2	ide cnt 1	ide cnt 0
7	6	5	4	3	2	1	0

After reset, it is initialized to 0x07ff.

Bits	Name	Description
15:12		Reserved.
11:0	idecnt	In master/dci mode, program this register to the sector size. In master mode, reading from this register will reveal the count down value.

Host Interface (host side) Registers

The following describes the host interface host side registers.

H_HOSTDMAPORT (0x0 16-bit R/W)

d							
15	14	13	12	11	10	9	8
d							
7	6	5	4	3	2	1	0

This register contains data transferred to/from the RISC. After reset, it is initialized to 0x0000.

H_HOSTVCXPORT (0x1 8-bit R/W)

d							
7	6	5	4	3	2	1	0

This register contains data transferred to/from the RISC. After reset, it is initialized to 0x00.

H_HOSTDBGPORT (0x2 8-bit R/W)

d							
7	6	5	4	3	2	1	0

This register contains data transferred to/from the RISC. After reset, it is initialized to 0x00.

H_HOSTCTL (0x3 8-bit R/W)

h2r irq	Isel 2	Isel 1	Isel 0	0sel 2	0sel 1	0sel 0	clr rirq
7	6	5	4	3	2	1	0

After reset, it is initialized to 0x00.

Bits	Name	Description
7	h2rirrq	Host to RISC IRQ. Writing a 1 to this bit sets the host to RISC IRQ flag.
6:1	Osel/Isel	Select which tre and dw bits are sent to the HRDREQ (read request) and HWRREQ (write request) pins. HRDREQ = (DmaDw & Osel0) | (VcxDw & Osel1) | (DbgDw & Osel2). HWRREQ = (DmaTre & Issel0) | (VcxTre & Isel1) | DbgTre & Isel2).
0	clrrirq	clear the r2hirq. Writing a 1 to this bit clears the RISC to host IRQ.

H_HOSTMASK (0x4, 8-bit, R/W)

endn sel	dbg tre	dbg dw	dma tre	dma dw	vcxi tre	vcxi dw	r2r irq
7	6	5	4	3	2	1	0

After reset, it is initialized to 0x00.

Bits	Name	Description
7	endnsel	Endian select; 1 = switch upper/lower bytes when write H_HOSTDMAPORT.
6:0		Mask bits for interrupts from the RISC to the host. This pin (HIRQ) is active high.

H_HOSTIRQSTAT (0x5, 8-bit, R)

h2r irq	dbg tre	dbg dw	dma tre	dma dw	vcxi tre	vcxi dw	r2h irq
7	6	5	4	3	2	1	0

This register reads the status of Interrupts from the RISC to the host; 1=IRQ, 0=no IRQ.

Bits	Name	Description
7	h2rirq	Interrupt flag set by the host as a signal to the RISC.
6	dbgtre	Debug transmit register empty (OK for host to send data to the RISC).
5	dbgdw	Debug data waiting (host needs to read data from the RISC).
4	dmatre	DMA transmit register empty (OK for host to send data to the RISC).
3	dmadw	DMA data waiting (host needs to read data from the RISC).
2	vcxitre	VCXI transmit register empty (OK for host to send data to the RISC).
1	vcxidw	VCXI data waiting (host needs to read data from the RISC).
0	r2hirq	Interrupt flag set by the RISC as a signal to the host.

DCI Interface

The following describes the DCI Interface registers.

R_HOSTCTL (0x2000300c 9-bit R/W)

x							dci en
15	14	13	12	11	10	9	8
dci edge	clr dirq	dci msk	dci mode	gw2 hst	hst2 xpt	r2h irq	clr hirq
7	6	5	4	3	2	1	0

R_HOSTCTL is a control register for the host. After reset, it is initialized to 0x10.

Note: By default, the chip is in DCI mode.
To program the chip to slave mode, set the dcimode bit of R_HOSTCTL TO 0.
To program the chip in master mode, first set the hstmode bit of R_IDECTL to 1, then set the dcimode bit of R_HOSTCTL to 0.

Bits	Name	Description
15:9	–	Reserved.
8	dcien	0 = sample data on rising edgeof dci clock. 1 = enable request to DVD-DSP chip.
7	dciedge	0 = sample data on rising edge of dci clock.
6	clrdirq	clear sector-end interrupt from DCI port to RISC.
5	dcimsk	mask sector-end interrupt from DCI port to RISC.
4	dcimode	0 = allows the host port to be configured as master or slave. 1 = hstmode bit of R_IDECTL set to 0, receive data from dvd-dsp.
3	gw2hst	0 = allows data transfer from RISC to host. 1 = allows data transfer from gateway to host.
2	hst2xpt	0 = allows data transfer to RISC. 1 = HST2XPT.
1	r2hirq	RISC to host IRQ. Writing a 1 to this bit sets the RISC to host IRQ flag.
0	clrhirq	clear host IRQ. Writing a 1 to this bit clears the host to RISC IRQ.

Audio Registers

Audio Interface Registers

This sub-section describes all the registers in audio. It serves as a reference for both hardware and firmware engineers who need to understand the internal workings of the chip.

AUDIODATA (0x2000d000 16-bit R/W)

d							
15	14	13	12	11	10	9	8
d							
7	6	5	4	3	2	1	0

This audio port data register is used for debug purpose only. Data is transferred to/from the audio block through this register. After reset, it is initialized to 0x0000.

AUDIOSTATUS (0x2000d004 8-bit R/W)

scse	cse	stre	sue	acse	aue	atre	adw
7	6	5	4	3	2	1	0

This Audio/SPDIF status register indicates the status/error in the audio block. Interrupt will be asserted upon any bit being set in this register provided that the corresponding interrupt is not masked. Write a “1” to clear the corresponding interrupt (except bit 6, which will be cleared upon the writing of register SPDIF_CSD1).

After reset, it is initialized to 0x00.:

Bits	Name	Description
7	SCSE	SPDIF channel swap error.
6	CSE	Channel status error.
5	STRE	SPDIF transmit register empty (spdif_tre).
4	SUE	SPDIF underflow error.
3	ACSE	Audio channel swap error.
2	AUE	Audio underflow error.
1	ATRE	Audio transmit register empty (au_tre).
0	ADW	Audio data waiting.

AUDIOCTL (0x2000d008 8-bit R/W)

aien	ams	aren	axen	aben	dm	srst	rsvd
7	6	5	4	3	2	1	0

This Audio Control register enables the corresponding functions and clocks. After reset, it is initialized to 0x00.

Bits	Name	Description
7	AIEN	Audio interrupt enable. The corresponding part must be enabled for proper interrupt status. 0 = disabled. 1 = enabled.
6	AMS	Audio master clock selection: 0 = external MCLK. 1 = internal MCLK.
5	AREN	Audio receive enable. 0 = disabled. 1 = enabled.
4	AXEN	Audio transmit enable. It is required that the DMA is started before enabling the transmit port.
3	ABEN	Audio bit clock generator enable (used only when internal MCLK is selected).
2	DM	Data input (either from pri_bus or risc) debug mode: 0 = data from pri_bus. 1 = data from risc_bus.
1	SRST	Soft reset, this bit will self-reset when a “1” is written.
0	rsvd	Reserved.

AUDIOXMT (0x2000d00c 16-bit R/W)

tlsb	tdge	tdfs	tdm			tcf	
15	14	13	12	11	10	9	8
tfm		itfs	tbcs	am		tbcf	
7	6	5	4	3	2	1	0

This Audio Transmit Format register is used for setting up the format for the transmit port. After reset, the register is initialized to 0x0000.

Bits	Name	Description
15	TLSB	0 = MSB first. 1 = LSB first.
14	TDGE	Bit clock edge for transmitting data: 0 = output data on rising edge. 1 = output data on falling edge.
13	TDFS	Data transmit sequence: 0 = first bit sent on first cycle. 1 = last bit sent on last cycle.
12:10	TDM	Transmit data mode: 000 = 16-bit data frame. 001 = 18-bit data frame. 010 = 20-bit data frame. 011 = 24-bit data frame. 100 = 32-bit data frame. 101 = reserved. 110 = reserved. 111 = reserved.
9:8	TCF	Transmit cycle frame: 00 = 16-bit cycle frame. 01 = 24-bit cycle frame. 10 = 32-bit cycle frame. 11 = reserved.
7:6	TFM	Transmit frame mode: 00 = normal mode. 01 = left justified mode. 10 = right justified mode. 11 = reserved.
5	ITFS	Inverse audio transmit frame sync. 0 = disabled. 1 = enabled.
4	TBCS	Bit clock select: 0 = use external bit clock. 1 = use internal bit clock and output bit clock.
3:2	AM	Audio Mode: 00 = Stereo L-R channel. 01 = reserved. 10 = reserved. 11 = reserved.
1:0	TBCF	Bit clock frequency select: 00 = MCLK/8. 01 = MCLK/4. 10 = MCLK/2. 11 = MCLK/16.

AUDIORCV (0x2000d010 16-bit R/W)

rlsb	rdge	rdfs	rsvd	rdm		rcf	
15	14	13	12	11	10	9	8
rfm		rfs	rbcs	rsvd	rsvd	rbcf	
7	6	5	4	3	2	1	0

This is the audio receive format register. After reset, it is initialized to 0x0000.

Bits	Name	Description
15	RLSB	0 = MSB first. 1 = LSB first
14	RDGE	Bit clock edge for receiving data. 0 = sample input data on rising edge. 1 = sample nput data on falling edge.
13	RDFS	Data receive sequence: 0 = first bit sent on first cycle. 1 = last bit sent on last cycle
11:10	RDM	Receive data frame: 00 = 16-bit data frame. 01 = reserved. 10 = reserved. 11 = reserved.
9:8	RCF	Receive cycle frame: 00 = 16-bit cycle frame. 01 = 24-bit cycle frame. 10 = 32-bit cycle frame. 11 = reserved.
7:6	RFM	Receive frame mode: 00 = normal mode (not supported). 01 = select frame mode, left justified mode. 10 = select frame mode, right justified mode. 11 = reserved.
5	IRFS	Inverse receive frame synch: 0 = disabled. 1 = enabled.
4	RBCS	Bit clock select: 0 = use external bit clock. 1 = use internal bit clock and output bit clock to pin.
3:2		reserved.
1:0	RBCF	Bit clock frequency select: 00 = MCLK/8. 01 = MCLK/4. 10 = MCLK/2. 11 = MCLK/1. Bit clock is generated by dividing the master clock with n selected.

AUDIOAPLLM (0x2000d014 8-bit R/W)

m							
7	6	5	4	3	2	1	0

This register is the Analog PLL Frequency Divider register. After reset, it is initialized to 0x4a.

Bits	Name	Description
7:0	m	Audio frequency divider M.

AUDIOAPLLN (0x2000d018 8-bit R/W)

fs							
7	6	5	4	3	2	1	0

This register is the Analog PLL Frequency Multiplier register. After reset, it is initialized to 0x1f.

Bits	Name	Description
7	FS	Sampling frequency selection: 0 = 256 fs. 1 = 384fs.
6:0	N	Audio frequency multiplier N.

S/PDIF Interface Registers

The following describes the S/PDIF interface registers.

SPDIF_CTL (0x2000d01c 8-bit R/W)

b							
7	6	5	4	3	2	1	0

After reset, it is initialized to 0x00.

Bits	Name	Description
7	–	Reserved.
6	B6	Soft reset.
5:4	B5,B4	Bit clock frequency select: 00 = SPMCLK/8 (n=8) 01 = SPMCLK/4 (n=2) 10 = SPMCLK/2 (n=4) 11 = SPMCLK/16 (n=16) Bit clock is generated by dividing the master clock with the n selected.
3	B3	Validity for subframe.
2	B2	User data bit for subframe.
1	B1	SPDIF input enable (not supported): 0 = disabled. 1 = enabled.
0	B0	SPDIF output enable: 0 = disabled. 1 = enabled.

SPDIF_CSD1 (0x2000d020 32-bit R/W)

cds1							
31	30	29	28	27	26	25	24
cds1							
23	22	21	20	19	18	17	16
cds1							
15	14	13	12	11	10	9	8
cds1							
7	6	5	4	3	2	1	0

This register is the SPDIF Channel Status 1 register. After reset, it is initialized to 0x0000 0000.

Bits	Name	Description
31:0	CDS1	SPDIF channel status data.

SPDIF_CSD2 (0x2000d024 32-bit R/W)

cds2							
31	30	29	28	27	26	25	24
cds2							
23	22	21	20	19	18	17	16
cds2							
15	14	13	12	11	10	9	8
cds2							
7	6	5	4	3	2	1	0

This register is the SPDIF Channel Status 2 register. After reset, it is initialized to 0x0000 0000.

Bits	Name	Description
31:0	CDS2	SPDIF channel status data.

SPDIF_CSD4 (0x2000d02c 32-bit R/W)

cds4							
31	30	29	28	27	26	25	24
cds4							
23	22	21	20	19	18	17	16
cds4							
15	14	13	12	11	10	9	8
cds4							
7	6	5	4	3	2	1	0

This register is the SPDIF Channel Status 4 register. After reset, it is initialized to 0x0000 0000.

Bits	Name	Description
31:0	CDS4	SPDIF channel status data.

SPDIF_CSD3 (0x2000d028 32-bit R/W)

cds3							
31	30	29	28	27	26	25	24
cds3							
23	22	21	20	19	18	17	16
cds3							
15	14	13	12	11	10	9	8
cds3							
7	6	5	4	3	2	1	0

This register is the SPDIF Channel Status 3 register. After reset, it is initialized to 0x0000 0000.

Bits	Name	Description
31:0	CDS3	SPDIF channel status data.

SPDIF_CSD5 (0x2000d030 32-bit R/W)

cds5							
31	30	29	28	27	26	25	24
cds5							
23	22	21	20	19	18	17	16
cds5							
15	14	13	12	11	10	9	8
cds5							
7	6	5	4	3	2	1	0

This register is the SPDIF Channel Status 5 register. After reset, it is initialized to 0x0000 0000.

Bits	Name	Description
31:0	CDS5	SPDIF channel status data.

SPDIF_CSD6 **(0x2000d034 32-bit R/W)**

cds6							
31	30	29	28	27	26	25	24
cds6							
23	22	21	20	19	18	17	16
cds6							
15	14	13	12	11	10	9	8
cds6							
7	6	5	4	3	2	1	0

This register is the SPDIF Channel Status 6 register. After reset, it is initialized to 0x0000 0000.

Bits	Name	Description
31:0	CDS6	SPDIF channel status data.

AUDIOIMASK **(0x2000d038 8-bit R/W)**

msse	mscse	mstre	msue	macs	maue	matre	madw
7	6	5	4	3	2	1	0

This register is the Audio Interrupt Mask register. After reset, it is initialized to 0x00. Write a “1” to the corresponding bit to mask the interrupt.

Bits	Name	Description
7	MSSE	Mask for SPDIF channel swap error.
6	MSCSE	Mask for SPDIF channel status empty.
5	MSTRE	Mask for SPDIF transmit register empty.
4	MSUE	Mask for SPDIF underflow error.
3	MACS	Mask for audio channel swap error.
2	MAUE	Mask for audio underflow error.
1	MATRE	Mask for audio transmit register empty.
0	MADW	Mask for audio data waiting interrupt.

Sub-Picture Unit (SPU) Related Registers

The following describes the Sub-Picture Unit (SPU) Related registers.

SP_SPCTL (0x20001600 10-bit R/W)

x						reset2	sp_rel
15	14	13	12	11	10	9	8
ccirq en	risc_ done	spuon	reset	rleat	dcseat	rlirqen	dcsirq en
7	6	5	4	3	2	1	0

This register is the Sub-Picture Control register. After reset, it is initialized to 0x000. Write a “1” to the corresponding bit to mask the interrupt.

Bits	Name	Description
15:10	-	Reserved.
9	RESET2	Write only: 1 = Reset part of SPU (i.e., similar to reset at the end of a frame); the FIFOs and the state machines are reset, but not the registers (one clock cycle). 0 = Nothing. Need to kill DMA and set this bit before every frame if DMA is not exact.
8	SP_REL	0 = Coordinates for changes within the Sub-Picture are relative to the main video display area. 1 = Coordinates for changes within the Sub-Picture are relative to the Sub-Picture.
7	CCIRQ_ EN	1 = Col/con command error interrupt enable. 0 = Disabled.
6	RISC_D ONE	Write only: 1 = RISC done with decoding SP (one clock cycle). 0 = Otherwise.
5	SPUON	Sub-Picture on/off: 1 = Sub-Picture is on. 0 = Sub-Picture is off.
4	RESET	Write only: 1 = Reset Sub-Picture unit (one clock cycle). 0 = Otherwise.
3	RLEAT	RISC eat RLFIFO: 0 = RISC read FIFO output only, no change in value. 1 = RISC read FIFO, causes it to eat byte.
2	DCSEAT	RISC eat DCSFIFO: 0 = RISC read FIFO output only, no change in value. 1 = RISC read FIFO, causes it to eat byte.
1	RLIRQE N	1 = RLFIFO IRQ enable. 0 = RLFIFO IRQ disable.
0	DCSIRQ EN	1 = DCSFIFO IRQ enable. 0 = DCSFIFO IRQ disable.

SP_VCNT (0x20001700 11-bit R/W)

x					d		
15	14	13	12	11	10	9	8
d							
7	6	5	4	3	2	1	0

This register is the Vertical Counter Value register. After reset, it is initialized to 0x7fe.

SP_VCNTREG (0x20001704 11-bit R/W)

x					d		
15	14	13	12	11	10	9	8
d							
7	6	5	4	3	2	1	0

This register is the Vertical Counter Initial Value register. After reset, it is initialized to 0x7fe.

SP_HCNT (0x20001708 11-bit R/W)

x					d		
15	14	13	12	11	10	9	8
d							
7	6	5	4	3	2	1	0

This register is the Horizontal Counter Value register. After reset, it is initialized to 0x0.

SP_HCNTREG (0x2000170C 11-bit R/W)

x					d		
15	14	13	12	11	10	9	8
d							
7	6	5	4	3	2	1	0

This register is the Horizontal Counter Initial Value register. After reset, it is initialized to 0x000.

SP_VSTART (0x20001710 10-bit R/W)
SP_VSTART is the Start Line of Sub-Picture register. After reset, it is initialized to 0x3FF.

SP_VEND (0x20001714 10-bit R/W)
SP_VEND is the End Line of Sub-Picture register. After reset, it is initialized to 0x3FF.

SP_HSTART (0x20001718 10-bit R/W)
SP_HSTART is the Horizontal Start Pixel of the Sub-Picture register. After reset, the contents of this register is initialized to 0x3FF.

SP_HEND (0x2000171C 10-bit R/W)
SP_HEND is the Start Line of Sub-Picture register. After reset, it is initialized to 0x3FF.

SP_SUBVCNT (0X20001720 10-bit R/W)
SP_SUBVCNT is the Line Number within the Sub-Picture register. After reset, it is initialized to 0x3FF.

SP_SUBHCNT (0X20001724 10-bit R/W)
SP_SUBHCNT is the Pixel Number within the Sub-Picture register. After reset, it is initialized to 0x3FF.

SP_VCSTART (0X20001728 10-bit R/W)
SP_VCSTART is the Start Line of Current Sub-Picture Change register. After reset, it is initialized to 0x3FF.

SP_VCEND (0X2000172C 10-bit R/W)
SP_VCEND is the End Line of Current Sub-Picture Change register. After reset, it is initialized to 0x3FF.

SP_HIVS (0X20001730 10-bit R/W)
SP_HIVS is the Hilite Start Line Number register. After reset, it is initialized to 0x3FF.

SP_HIVE (0X20001734 10-bit R/W)
SP_HIVE is the Hilite End Line Number register. After reset, it is initialized to 0x3FF.

SP_HIHS (0X20001738 10-bit R/W)
SP_HIHS is the Hilite Start Pixel Number register. After reset, it is initialized to 0x3FF.

SP_HIHE (0X2000173c 10-bit R/W)
SP_HIHE is the Hilite End Pixel Number register. After reset, it is initialized to 0x3FF.

SP_HSTART1 (0X20001740 10-bit R/W)
SP_HSTART2 (0X20001744 10-bit R/W)
SP_HSTART3 (0X20001748 10-bit R/W)
SP_HSTART4 (0X2000174C 10-bit R/W)
SP_HSTART5 (0X20001750 10-bit R/W)
SP_HSTART6 (0X20001754 10-bit R/W)
SP_HSTART7 (0X20001758 10-bit R/W)
SP_HSTART8 (0X2000175C 10-bit R/W)
SP_HSTART [8:1] are the Pixel Number for Start of Changes 1 Through 8 register. After reset, the contents of these registers are initialized to 0x3FF.

x						d	
15	14	13	12	11	10	9	8
d							
7	6	5	4	3	2	1	0

NOTE: The register bit tables for all these registers are identical to the one shown above.

SP_VTCTL (0x20001760 16-bit R/W)

numchg				cindex			
15	14	13	12	11	10	9	8
cs				cc par seen	rl en	chg val id	hi val id
7	6	5	4	3	2	1	0

This register is the Video Timing Control register. After reset, it is initialized to 0x0000.

Bits	Name	Description
15:12	NUMCHG [3:0]	Number of changes in current horizontal stripe.
11:8	CINDEX	Code index (current region index).
7:4	CS	Current state of COL/CON state machine (read only).
3	CCPA_ SEEN	1 = Start parsing COL/CON data (one clock cycle) (need to set after RISC decodes). 0 = Otherwise.
2	RLEN	1 = Current pixel in Sub-Picture display area. 0 = Otherwise.
1	chg val id	1 = Current pixel is within a change region (i.e., not default Sub-Picture color/contrast). 0 = Otherwise.
0	hi val id	1 = Current pixel is within the hilight region. 2 = Otherwise.

SP_CON0 (0x200017b0-17d4 16-bit R/W)
SP_CON0 through SP_CON9 are registers containing the contrast index for a particular region and pixel type.

CON0 is the default Sub-Picture region register.

After reset, it is initialized to 0x0000.

SP_CON1 (0x200017b4 16-bit R/W)
SP_CON2 (0x200017b8 16-bit R/W)
SP_CON3 (0x200017bc 16-bit R/W)
SP_CON4 (0x200017c0 16-bit R/W)
SP_CON5 (0x200017c4 16-bit R/W)
SP_CON6 (0x200017c8 16-bit R/W)
SP_CON7 (0x200017cc 16-bit R/W)
SP_CON8 (0x200017d0 16-bit R/W)
SP_CON0 through SP_CON9 are registers containing the contrast index for a particular region and pixel type.

CON1 though CON8 are the change region registers.

After reset, it is initialized to 0x0000.

SP_CON9 (0x200017d4 16-bit R/W)
SP_CON0 through SP_CON9 are registers containing the contrast index for a particular region and pixel type.

CON9 is the hi-lite region register.

After reset, it is initialized to 0x0000.

d				c			
15	14	13	12	11	10	9	8
b				a			
7	6	5	4	3	2	1	0

NOTE: The register bit tables for all these registers are identical to the one shown above.

Color Index Registers

The following describes the Color Index registers.

SP_COL0 (0x20001780 16-bit R/W)
SP_COL0 through SP_COL9 are registers containing color index for a particular region and pixel type.

COL0 is the default Sub-Picture region register.

After reset, it is initialized to 0x0000.

SP_COL1 (0x20001784 16-bit R/W)
SP_COL2 (0x20001784 16-bit R/W)
SP_COL3 (0x2000178C 16-bit R/W)
SP_COL4 (0x20001790 16-bit R/W)
SP_COL5 (0x20001794 16-bit R/W)
SP_COL6 (0x20001798 16-bit R/W)
SP_COL7 (0x2000178C 16-bit R/W)
SP_COL8 (0x200017A0 16-bit R/W)
SP_COL0 through SP_COL9 are registers containing color index for a particular region and pixel type.

COL1-8 are the change region 1-8 registers.

After reset, it is initialized to 0x0000.

SP_COL9 (0x200017A4 16-bit R/W)
SP_COL0 through SP_COL9 are registers containing color index for a particular region and pixel type.

COL9 is the highlight region register.

After reset, it is initialized to 0x0000.

d				c			
15	14	13	12	11	10	9	8
b				a			
7	6	5	4	3	2	1	0

NOTE: The register bit tables for all these registers are identical to the one shown above.

Bits	Name	Description
15:12	D[3:0]	Color index for emphasis 2 pixel (type 11).
11:0	C[3:0]	Color index for emphasis 1 pixel (type 10).
7:4	B[3:0]	Color index for pattern pixel (type 01).
3:0	A[3:0]	Color index for background pixel (type 00).

Video Interface Registers

The following describes the video interface registers.

Video (Output) Registers

Video timing for the output (screen) section is shown in Figure 23. All screen location values are given in pixels.

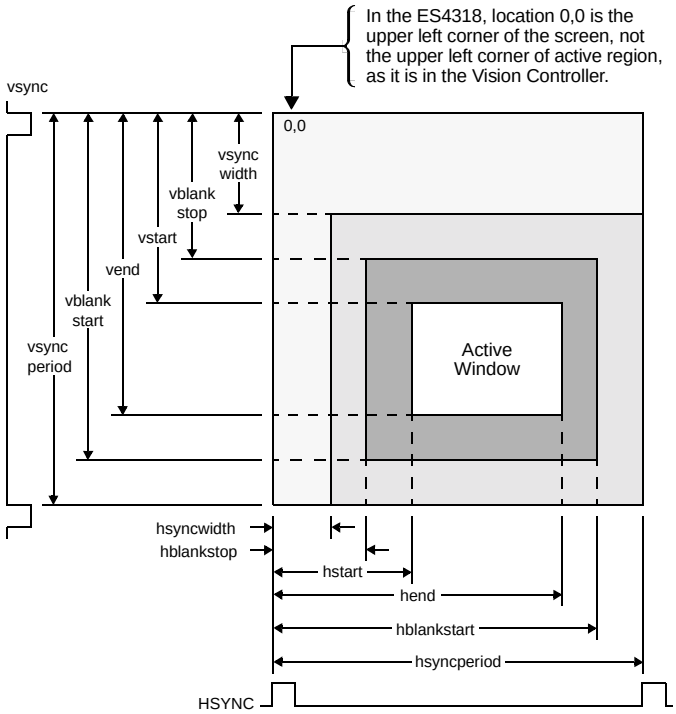


Figure 23 Video Output Timing

VID_SCN_HSTART (20001000h, 13-bit, W)

x			hstart				
15	14	13	12	11	10	9	8
hstart							
7	6	5	4	3	2	1	0

This register contains the horizontal starting address of the active window for the screen.

Bits	Name	Description
15:13	–	Reserved.
12:0	hstart	Horizontal start of active window. See Figure 23.

VID_SCN_HEND (20001004h, 13-bit, W)

x			hend				
15	14	13	12	11	10	9	8
hend							
7	6	5	4	3	2	1	0

This register contains the horizontal ending address of the active window for the screen.

Bits	Name	Description
15:13	–	Reserved.
12:0	hend	Horizontal end of active window. See Figure 23.

VID_SCN_VSTART (20001008h, 13-bit, W)

x			vstart				
15	14	13	12	11	10	9	8
vstart							
7	6	5	4	3	2	1	0

This register contains the vertical starting address of the active window for the screen.

Bits	Name	Description
15:13	–	Reserved.
12:0	vstart	Vertical start of active window. See Figure 23.

VID_SCN_VEND (2000100ch, 13-bit, W)

x			vend				
15	14	13	12	11	10	9	8
vend							
7	6	5	4	3	2	1	0

This register contains the vertical ending address of the active window for the screen.

Bits	Name	Description
15:13	–	Reserved.
12:0	vend	Vertical end of active window.

VID_SCN_VERTIRQ (20001010h, 13-bit, W)

x			vertirq				
15	14	13	12	11	10	9	8
vertirq							
7	6	5	4	3	2	1	0

This register is selectable by software and contains the line in which a vertical interrupt will occur. Line 0 is the top of the screen (leading edge of VSYNC pin). Typical is to set an interrupt either just before or just after the active region of the screen.

Bits	Name	Description
15:13	–	Reserved.
12:0	vertirq	Line where a vertical interrupt will occur.

VID_SCN_HBLANK_START (20001014h, 13-bit, W)

x			hblankstart				
15	14	13	12	11	10	9	8
hblankstart							
7	6	5	4	3	2	1	0

This register contains the starting address of the horizontal blanking.

Bits	Name	Description
15:13	–	Reserved.
12:0	hblankstart	Start of horizontal blanking. See Figure 23.

VID_SCN_HBLANK_STOP (20001018h, 13-bit, W)

x			hblanksto				
15	14	13	12	11	10	9	8
hblanksto							
7	6	5	4	3	2	1	0

This register contains the ending address of the horizontal blanking.

Bits	Name	Description
15:13	–	Reserved.
12:0	hblankstop	End of horizontal blanking. See Figure 23.

VID_SCN_VBLANK_START (2000101ch, 13-bit, W)

x			vblankstart				
15	14	13	12	11	10	9	8
vblankstart							
7	6	5	4	3	2	1	0

This register contains the starting address of the vertical blanking.

Bits	Name	Description
15:13	–	Reserved.
12:0	vblankstart	Start of vertical blanking. See Figure 23.

VID_SCN_VBLANK_STOP (20001020h, 13-bit, W)

x			vblankstop				
15	14	13	12	11	10	9	8
vblankstop							
7	6	5	4	3	2	1	0

This register contains the ending address of the vertical blanking.

Bits	Name	Description
15:13	–	Reserved.
12:0	vblankstop	End of vertical blanking. See Figure 23.

VID_SCN_HSYNCWIDTH (20001024h, 13-bit, W)

x			hsyncwidth				
15	14	13	12	11	10	9	8
hsyncwidth							
7	6	5	4	3	2	1	0

This register contains the width of the horizontal sync pulse. It is needed only if sync direction is output. (MVD drives the HSYNC pin.)

Bits	Name	Description
15:13	–	Reserved.
12:0	hsyncwidth	Horizontal sync pulse width. See Figure 23.

VID_SCN_HSYNCPERIOD (20001028h, 13-bit, W)

x			hsyncperiod				
15	14	13	12	11	10	9	8
hsyncperiod							
7	6	5	4	3	2	1	0

This register contains the period of the horizontal sync pulse. It is needed only if sync direction is output. (MVD drives the HSYNC pin.)

Bits	Name	Description
15:13	–	Reserved.
12:0	hsyncperiod	Horizontal sync period. See Figure 23.

VID_SCN_VSYNCPERIOD (2000102ch, 13-bit, W)

x			vsyncperiod				
15	14	13	12	11	10	9	8
vsyncperiod							
7	6	5	4	3	2	1	0

This register contains the period of the vertical sync pulse. It is needed only if sync direction is output. (MVD drives the VSYNC pin.)

Bits	Name	Description
15:13	–	Reserved.
12:0	vsyncperiod	Vertical sync pulse period. See Figure 23.

VID_SCN_VSYNCPIXEL (20001030h, 13-bit, W)

x			vsyncpixel				
15	14	13	12	11	10	9	8
vsyncpixel							
7	6	5	4	3	2	1	0

This register defines which pixel VSYNC will change on. The number of pixels delayed from HSYNC that VSYNC will change on (rise or fall). This is needed only if sync direction is output. (MVD drives the VSYNC pin.)

Bits	Name	Description
15:13	–	Reserved.
12:0	vsyncpixel	Pixel on which VSYNC will change. See Figure 23.

VID_SCN_VSYNCWIDTH (20001038h, 6-bit, W)

x		vsyncwidth					
7	6	5	4	3	2	1	0

This register defines the width of the vertical sync pulse. It is needed only if sync direction is output. (MVD drives the VSYNC pin.)

Bits	Name	Description
7:6	–	Reserved.
5:0	vsyncwidth	Vertical sync pulse width. This is needed only if sync direction is output. See Figure 23.

VID_SCN_COUNTER_CTL (2000103ch, 5-bit, W)

x			invblnk	0	invhs	invvs	master mode
7	6	5	4	3	2	1	0

This register contains miscellaneous counter control bits. After reset, it is initialized to 0x00.

Bits	Name	Description
7:5	–	Reserved.
4	invblnk	Inverted blank sync. 1 = blank is active low. 0 = otherwise.
3	–	Set at zero.
2	invhs	Inverted horizontal sync. 1 = horizontal sync is active low.
1	invvs	Inverted vertical sync. 1 = vertical sync is active low. 0 = otherwise.
0	master mode	0= syncs inputs to MVD. 1= MVD drives sync pins.

VID_SCN_HORIZCOUNT (20001040h, 13-bit, R)

x			horizcount				
15	14	13	12	11	10	9	8
horizcount							
7	6	5	4	3	2	1	0

For testing only. This register contains the current pixel of the horizontal counter. Starts at pixel 0 (the pixel at HSYNC).

Bits	Name	Description
15:13	–	Reserved.
12:0	horizcount	Current pixel of the horizontal counter.

VID_SCN_VERTCOUNT (20001044h, 13-bit, R)

x			vertcount				
15	14	13	12	11	10	9	8
vertcount							
7	6	5	4	3	2	1	0

For testing only. This register contains the current line of the vertical counter. Starts at line 0 (the line at VSYNC).

Bits	Name	Description
15:13	–	Reserved.
12:0	vertcount	Current pixel of the vertical counter.

VID_SCN_OUTPUTCNTL (20001100h, 16-bit, W)

x							
31	30	29	28	27	26	25	24
x							yuv 8-bit mode
23	22	21	20	19	18	17	16
pix_clk_sel	en phase DET	clk1x mod	clk_div1	clk_div0	yuv swap	invclkq	invrmsb
15	14	13	12	11	10	9	8
inv gmsb	inv bmsb	avg chrm	colrmod	x	cntrclr	clrvcnt	clrhcnt
7	6	5	4	3	2	1	0

This register contains the mode bits used to control video output.

Bits	Name	Description
31:17	–	Reserved.
16	yuv 8-bit mode	Use UV ports (8-bit) to send out Y and UV. 0 = Use Y port for Y and UV port for UV. 1 = Use UV port for Y, U, and V.
15	pix_clk_sel	Pixel_Clock source selecting: 0 = External source clock from pin CLK2XSCN. (default). 1 = Internal source clock from PLL (DCXO).
14	–	Enable the 13.5 MHz phase detection logic. This logic edtects the phase of the 13.5 MHz clock used inside the Brooktree chip. 0 = UV is selected first (default). 1 = Y is selected first. Valid only in ES3210 and later versions.
13	clk1xmod	In this mode, the Pixel_Clock is a 1x clk and the pin CLKQSCN is not used. 0 = use PADCLKQSCN (13.5 MHz). 1 = use PADCLK2XSCN (27 MHz).
12:11	clk_div	00 = Screen clock depends on clk1xmod pin (default). 01 = Screen clock frequency is half of input Pixel_Clock (13.5 MHz). 1x = Screen clock frequency is a quarter of input Pixel_Clock (6.75 MHz).
10	yuv swap	0 = UV is selected first. 1 = Y is selected first.
9	invclkqc	Invert the CLKQS pin (PADCLKSCN).
8	invrmsb	Invert bit 7 of R. (Also UV when in YUV422, and U when yuv444 mode.)
7	invgmsb	Invert bit 7 of G. (Y when in YUV4xx mode.)
6	invbmsb	Invert bit 7 of B. (V when in YUV444 mode.)
5	avgchrm	Average chroma enable. (For YUV422 to YUV444 module.) 0 = use (0.25u1 + 0.75u2). 1 = use simple average ((u1+u2)/2).
4	colrmod	Select the type of output color: 0 = YUV422, 16 bits. (default). 1 = RGB444, 16 bits.
3	–	Reserved.
2	cntrclr	Clear counter internal bits. This bit is set to level (set to 1 then set to 0).
1	clrvcnt	Clear the vertical counter. This bit is set to level (set to 1 then set to 0).
0	clrhcnt	Clear the horizontal counter. This bit is set to level (set to 1 then set to 0).

VID_SCN_OUTPUTSTATUS (20001104h, 6-bit, R)

x		odd_ even	blnk	hs	vs	13.5 mhz phs	actv
7	6	5	4	3	2	1	0

This register contains the status bits for the video section.

Bits	Name	Description
7:6	–	Reserved.
5	odd_even	Status of the vs/hs relationship to determine odd or even field useful when MVD is used as a slave of external video encoder.
4	blnk	status of internal blanking.
3	hs	Status of internal horizontal sync.
2	vs	Status of internal vertical sync.
1	13.5mhs_ phs	The phase of the 13.5 MHz clock used inside the Brooktree chip. Valid only in ES3210 and later versions.
0	actv	Set if in the active window.

VID_SCN_OSD_HSTART (20001110h, 13-bit, R/W)

x			hstart				
15	14	13	12	11	10	9	8
hstart							
7	6	5	4	3	2	1	0

This register contains the horizontal starting address (referenced from active window).

Bits	Name	Description
15:13	–	Reserved.
12:0	hstart	Horizontal starting address. See Figure 23.

VID_SCN_OSD_HEND (20001114h, 13-bit, R/W)

x			hend				
15	14	13	12	11	10	9	8
hend							
7	6	5	4	3	2	1	0

This register contains the horizontal ending address (referenced from active window).

Bits	Name	Description
15:13	–	Reserved.
12:0	hend	Horizontal ending address. See Figure 23.

VID_SCN_OSD_VSTART (20001118h, 13-bit, R/W)

x			vstart				
15	14	13	12	11	10	9	8
vstart							
7	6	5	4	3	2	1	0

This register contains the vertical starting address (referenced from active window).

Bits	Name	Description
15:13	–	Reserved.
12:0	vstart	Vertical starting address. See Figure 23.

VID_SCN_RESET (20001200h, 7-bit, R/W)

x	dmago	cirvirq	clrerrs	rsty	rstuv	rstsync	rstfrmt
7	6	5	4	3	2	1	0

Resets for the video screen section. These bits are set to 1 on reset.

Bits	Name	Description
7	–	Reserved.
6	dmago	DMA Go. (Start new field). 1 = reset everything (FIFOs, etc.). 0 = start DMA. At bottom of screen DMA will stop until another dmago is asserted.
5	clrvirq	Clear the virq bit.
4	clrerrs	Clear the IRQ status bits.
3	rsty	Reset the Y screen section for video screen section.
2	rstuv	Reset the UV screen section (including Y FIFO control).
1	rstsync	Reset the “SyncBlock” state machine.
0	rstfrmt	Reset the output formatter.

VID_SCN_MISC1 (20001224h, 18-bit, R/W)

x							
31	30	29	28	27	26	25	24
x						bytestrty1	bytestrty0
23	22	21	20	19	18	17	16
bytestrtu1	bytestrtu0	bytestrtv1	bytestrtv0	ltrboxen	virqmsk	zeroy1st	ilacyen
15	14	13	12	11	10	9	8
avgyilac	errmsk	uvalu1	x	invyalu	zerouv1st	tablload	invuvalu
7	6	5	4	3	2	1	0

This register contains the mode bits that control the video output.

Bits	Name	Description
31:18	–	Reserved.
17	bytestrty1	Byte starting position for y data pan/scan operation. * see table below.
16	bytestrty0	Byte starting position for y data pan/scan operation. * see table below.
16	bytestrtu1	Byte starting position for u data pan/scan operation. * see table below.
14	bytestrtu0	Byte starting position for u data pan/scan operation. * see table below.
13	bytestrtv1	Byte starting position for v data pan/scan operation. * see table below.
12	bytestrtv0	Byte starting position for v data pan/scan operation. * Table. 00 = byte, xx, xx, xx. 01 = xx, byte, xx, xx 10 = xx, xx, byte, xx 11 = xx, xx, xx, byte
11	ltrboxen	0 = There is nothing to change in the active region (default). 1 = Letter box enable. The active screen will blank out on top and bottom according to the value set in the registers: VID_SCN_VBLANK_START and VID_SCN_VBLANK_STOP.
10	virqmsk	Interrupt mask for virq.
9	zeroy1st	0 = top line will be interlaced with itself. 1 = top line will be interlaced with zeros.
8	ilacyen	Interlace enable bit.
7	avgyilac	When this bit is enabled, interlacing will be 1/2,1/2, not 3/4, 1/4.
6	errmsk	Interrupt mask for YFIFO underflow error.
5	uvalu1	Selects the interpolation/interlace values to use: 0 = 3/4, 1/4. 1 = 1/2, 1/2.
4	–	Reserved.
3	invyalu	When interlacing is enabled, this bit selects whether the first line is 1/4 or 3/4 0 = 1/4n + 3/4(n+1). 1 = 3/4n + 1/4(n+1).
2	zerouv1st	1 = top line will be interpolated with zeros. 0 = top line will be interpolated with itself.
1	tablload	Set this bit when loading the Noise Reduction and Filter Table RAM.
0	invuvalu	Set this bit to the same value as bit 5 (uvalu1).

VID_SCN_OSD_VEND (2000111ch, 13-bit, R/W)

x			vend				
15	14	13	12	11	10	9	8
vend							
7	6	5	4	3	2	1	0

This register contains the vertical ending address (referenced from active window).

Restriction: The OSD window must be smaller than the active window. Namely:
(VID_SCN_OSD_HEND - VID_SCN_OSD_HSTART)
<
(VID_SCN_HEND - VID_SCN_HSTART)
and
(VID_SCN_OSD_VEND - VID_SCN_OSD_VSTART)
<
(VID_SCN_VEND - VID_SCN_VSTART)

Bits	Name	Description
15:13	–	Reserved.
12:0	vend	Vertical ending address. See Figure 23.

VID_SCN_OSD_MISC (20001124h, 8-bit, R/W)

lat_int	reset_ overlay	pal_index		inten	idmd	mode	
7	6	5	4	3	2	1	0

This register contains miscellaneous control and status bits.

Bits	Name	Description
7	lat_int	Latched interrupt. This is a read-only bit.
6	reset_overlay	Reset overlay section (set to 1 at reset).
5:4	pal_index	Upper 2 bits of palette address when in 2-bit mode.
3	inten	Interrupt enable.
2	ldmd	Enable palette load.
1:0	mode	0 0 = Bypass (initializes to 00 at reset). 0 1 = 2 bit/pixel. 1 0 = 4 bit/pixel. 1 1 = 8 bit/pixel.

VID_SCN_OSD_PALETTE
(20001140h–2000117ch, 16-bit, R/W)

y				v			
15	14	13	12	11	10	9	8
u				bin_on/ of	blnd		
7	6	5	4	3	2	1	0

These 16 registers contain the OSD palette.

Bits	Name	Description
15:12	y	Upper 4 bits of luminance data (lower 4 bits are 0).
11:8	v	Upper 4 bits of V chrominance data (lower 4 bits are 0).
7:4	u	Upper 4 bits of U chrominance data (lower 4 bits are 0).
3	blnd_on/off	0 = blending (transparency is off).
2:0	blnd	Blending value: value blnd value blnd 0 1/8 4 5/8 1 2/8 5 6/8 2 3/8 6 7/8 3 4/8 7 8/8 finalpixel = blnd x palette value + (1 - blnd) x original pixel.

NOTE: For mode 3 (8-bit/pixel) the upper 4 bits of the pixel are the blend information, the lower 4 bits are the palette index and the blend information in the palette is ignored.

Bus Control & DRAM Registers

The following describes bus control and DRAM registers.

BUSCON_DRAM_CONTROL (20008100h, 14-bit, R/W)

x		sdcfg2	sdcfg1	sdcfg0	srefen	refen	x
15	14	13	12	11	10	9	8
x		raspre1	raspre0	rasdel1	rasdel0	spd1	spd0
7	6	5	4	3	2	1	0

This is the configuration register for the reference memory DRAM. After reset, it is initialized to 0x0000.

Bits	Name	Description
15:14	–	Reserved.
13:11	sdcf	Configure the SDRAM & EDO memory. See Table 1 for details.
10	srefen	SDRAM refresh Enable. This bit is set to enable the refresh logic for SDRAM.
9	refen	Refresh Enable. This bit is set to enable the refresh logic for EDO DRAM.
8:6	–	Reserved.
5:4	raspre	RAS precharge for EDO/FP. raspre[1:0] - RAS Precharge time control raspre[1:0] DRAS precharge Time (trp) 03T(3* 1/frequency) 14T(4* 1/frequency) 25T(5* 1/frequency) Limitation - Use 5T only if spd is set to 2T.
3:2	rasdel	RAS delay for EDO/FP. rasdel[1:0] - RAS to CAS delay time control rasdel[1:0] DRAS to CAS delay time (trcd) 02T(3* 1/frequency) 13T(4* 1/frequency) 24T(5* 1/frequency) Limitation - Use 3T only if spd is set to 2T
1:0	spd	DRAM speed control: These control the speed of the DRAM interface signal in terms of the system cycle time (T). spd[1:0] fast page mode cycle time (tpc) 02T(30ns at 66MHz) (25ns at 80MHz) 13T(45ns at 66MHz) (37.5ns at 80MHz) 24T(60ns at 66MHz) (50ns at 80MHz) (2T high/low) 36T(90ns at 66MHz) (75ns at 80MHz) (for 16bit at 3t.)

BUSCON_DRAM_REFTIME (20008104h, 8-bit, R/W)

intval7	intval6	intval5	intval4	intval3	intval2	intval1	intval0
7	6	5	4	3	2	1	0

This register controls the refresh period for the system, and contains the refresh interval value. After reset, it is not initialized.

Bits	Name	Description
7:0	intval	Refresh interval value. Refresh Interval = (2048 - (t[7:0] x 8)) x 12.5 (for 80 MHz). Set t[7:0] = 99 (0x63) for memories which require 512 cycles per 8 msec. (This is 15 µsec per cycle.)

BUSCON_DRAM_SREFTIME (20008114h, 8-bit, R/W)

intval7	intval6	intval5	intval4	intval3	intval2	intval1	intval0
7	6	5	4	3	2	1	0

This register controls the SRAM refresh period for the system, and contains the refresh interval value. After reset, it is not initialized.

Bits	Name	Description
7:0	intval	Refresh interval value. Refresh Interval = (2048 - (t[7:0] x 8)) x 12.5 (for 80 MHz). Set t[7:0] = 99 (0x63) for memories which require 512 cycles per 8 msec. (This is 15 µsec per cycle.)

RISC Interface Registers

The following describes the RISC Interface registers.

RIFACE_WAIT_STATE (20004004h, 20-bit, R/W)

x							
31	30	29	28	27	26	25	24
x				bank3			
23	22	21	20	19	18	17	16
bank3	bank2					bank1	
15	14	13	12	11	10	9	8
bank1			bank0				
7	6	5	4	3	2	1	0

This register contains the number of external wait states (from 0 to 32) per access for banks 0-3. The table below gives the hexadecimal value for the number of wait states:

Hex Value	Wait State	Hex Value	Wait State	Hex Value	Wait State	Hex Value	Wait State
1F	0	17	8	0F	16	07	24
1E	1	16	9	0E	17	06	25
1D	2	15	10	0D	18	05	26
1C	3	14	11	0C	19	04	27
1B	4	13	12	0B	20	03	28
1A	5	12	13	0A	21	02	29
19	6	11	14	09	22	01	30
18	7	10	15	08	23	00	32 (default)

RIFACE_TURNOFF_DELAY (20004008h, 8-bit, R/W)

bank3 t		bank2 t		bank1 t		bank0 t	
7	6	5	4	3	2	1	0

This register contains the delay that occurred when switching from one bank to another. This register is used for devices with slow turnoff output enables (such as EPROMs).

Bits	Name	Description
7:0	banks 3-0 t	Turn off delay for banks 3-0: 00h = 3 T delay (default). 01h = 2 T delay. 10h = 1 T delay (at 80 MHz input clock, 1T = 12.5ns). 11h = 0 T delay.

NOTE: Delay turnoff only in effect when switching from 1 external bank access to another external bank access.

RIFACE_AUX1 (2000402ch, 10-bit, R/W)

x						e2 flag	d2 flag
15	14	13	12	11	10	9	8
e flag	d flag	t3	t2	p3	p2	p1	p0
7	6	5	4	3	2	1	0

This register is a general I/O port for interfacing with external devices. Possible uses:

1. IRQ to a 2101 DSP.
2. I²C bus to Phillips chips.
3. Auxiliary bits to external video logic.

Bits	Name	Description
15:10	–	Reserved.
9:6	e2 flag, d2 flag, e flag, d flag	General-purpose status flag. See the Operation paragraph immediately following this table for details.
5:4	t3, t2	Tri-state controls.
3	p3	Tri-stateable pad.
2	p2	Tri-stateable pad.
1	p1	Open collector pad.
0	p0	Open collector pad.

Operation:

When this register is read, the values read are the values at the PAD:

PadP3 = Tri-state(.D(P3), .OE(T3))
PadP2 = Tri-state(.D(P2), .OE(T2))
PadP1 = OpenCollector(.D(P1))
PadP0 = OpenCollector(.D(P0))

The two open collector pins allow I²C bus communication (They require an external pull-up resistor). The default value is for p3, p2 to be tri-state, and p1, p0 to be disabled (i.e., P1, P0 = high (logic 1), and T3, T2 = low (logic 0)).

NOTE: P3, P2 are multi-purpose pins, which can be reconfigured as follows:

E	D	P3 function
0	0	P3 (default).
0	1	DMA/RISCess flag (1 = DMA).
1	0	VPSTAT[4] vp data bus busy.
1	1	RISCess Inst/Data flag (1 = inst).

E2	D2	P2 function
0	0	p2 (default).
0	1	vpstat[2] VP I/O busy.
1	0	Buscon cmdque empty flag (before it is at p3). 1 means vpcmdq is empty.
1	1	VP cmdqempty, direct from cmdq count. P2 will be driven by bit [14] of the cmdq output.

NOTE: The e, d, e2, and d2 bits are write-only. They cannot be read.

RIFACE_AUX2 **(20004030h, 9-bit, R/W)**

x							aux7_ is_stall
15	14	13	12	11	10	9	8
t				p			
7	6	5	4	3	2	1	0

This register is a second general-purpose I/O port with four tri-state channels.

Bits	Name	Description
15:9	–	Reserved.
8	aux7_is_stall	RISCess stalled flag.
7:4	t[7:4]	Tri-stateable pads.
3:0	p[7:4]	Tri-state controls.

Operation:

When this register is read, the values read are the values at the PAD:

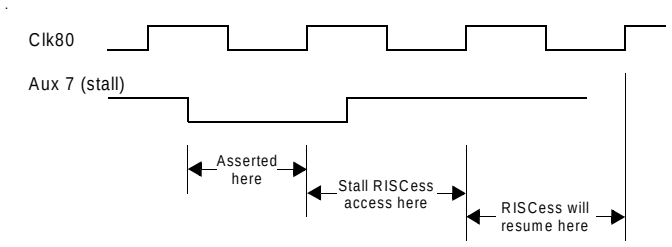
PadP7 = Tri-state(.D(P7), .OE(T7))
PadP6 = Tri-state(.D(P6), .OE(T6))
PadP5 = Tri-state(.D(P5), .OE(T5))
PadP4 = Tri-state(.D(P4), .OE(T4))

NOTE: Default values for tri-state controls are 0 (tri-state) at reset.

AUX7_is_stall Flag Operation:

RISCess can now be stalled externally via the AUX7 port. To configure this port, the aux7_is_stall flag must be set in the RIFACE_AUX2 register (this flag defaults to 0). When set, the AUX7 (P7) pin loses its AUX pin functionality, and becomes the RISCess STALL# pin.

STALL# is asserted active low, prior to the rising edge of DCI_CLK. The RISCess will be stalled the NEXT cycle.



NOTE: For busy-holdoff operations (for instance, where RISCess is accessing a microprocessor which is not ready yet, the external device cannot be accessed at 0-wait state, since there is a 1 cycle latency for the stall to take effect.

(SRAM Interface)

The following section describes the RISC Interface block.

RIFACE_WIDTH **(20004000h, 11-bit, R/W)**

x					dbg-mode	cache fls	cache disable
15	14	13	12	11	10	9	8
div2	div1	div0	b3w	b2w	b1w	b0w1	b0w0
7	6	5	4	3	2	1	0

This register contains the width of bus to external memory, internal RAM disable signal.

Bits	Name	Description
15:11	–	Reserved.
10	dbgmode	Debug mode: 0 = Save power from outside pins toggling. 1 = riscaddr and riscbus are seen from the SRAM address/data. Resets to 1.
9	cache fls	Cache flush: 1 = flush. Resets to 1.
8	cache disable	Cache disable signal: 0 = Cache enabled. 1 = Cache bypassed. Resets to 1 (Cache disabled).
7:5		
4:0	b3w b2w b1w b0w1 b0w0	w{1:0] = width (from 8,16,32): 00 = 8-bit wide (default). 01 = 16-bit wide. 10 = Undefined except for bank0, Bank 0 has a special mode: Map bank0 to DRAM. 11 = Undefined.

Two new function bits have been added to the TDMTSC# and TDMDX pins to help standalone systems boot.

TDMDX/RSEL	Selection
0	8-bit ROM.
1	16-bit ROM.

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Storage temperature range	-65° C to 150° C
Operating temperature range	-65° C to 110° C
Voltage range on any pin	-0.5 V to (VDD + 0.5 V)
Power dissipation	1.7 W

Recommended Operating Conditions

Operating temperature range	0° C to 70° C
Supply voltage VDD	3.65 V ± 150 mv
Supply voltage VPP	VPP is not necessary at 5V. VPP should always be: VDD <= VPP <= 5.5V See AppNote 2.

Stress beyond those listed under the Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the Recommended Operating Conditions section of this specification is not implied. Exposure to the Absolute Maximum Ratings conditions for extended periods may affect device reliability.

DC Electrical Characteristics

(Over recommended operating conditions)

Table 7 DC Electrical Characteristics

Symbol	Parameter	Min	Max	Unit	Comments
VIH	High-level input voltage	2.0	VDD+0.25	V	All inputs TTL levels except CLK
VIl	Low-level input voltage	-0.3	0.8	V	All inputs TTL levels except CLK
VCH	CLK high-level input	2.0	VDD+0.25	V	TTL level input
VCL	CLK low-level input	-0.3	0.8	V	TTL level input
VOH	High-level output voltage	3.0	–	V	IOH = 1 mA
VOL	Low-level output voltage	–	0.45	V	IOL = 4 mA
ILI	Input leakage current	–	±15	µA	
ILO	Output leakage current	–	±15	µA	
CIN	Input capacitance	–	10	pF	fc = 1 MHz
CO	Input/output capacitance	–	12	pF	fc = 1 MHz
CCLK	CLK capacitance	–	20	pF	fc = 1 MHz

AC Electrical Characteristics

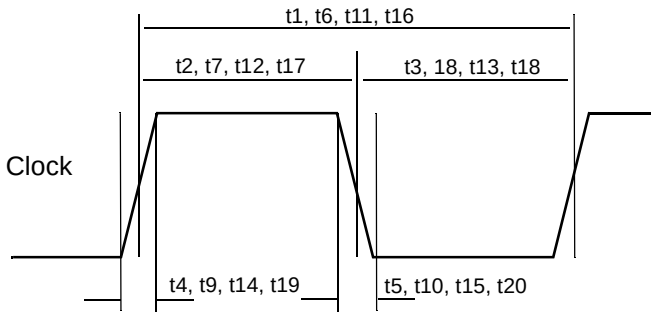


Figure 24 Swan-2™ ES4318 Clock Timing Diagram

Clock Timings

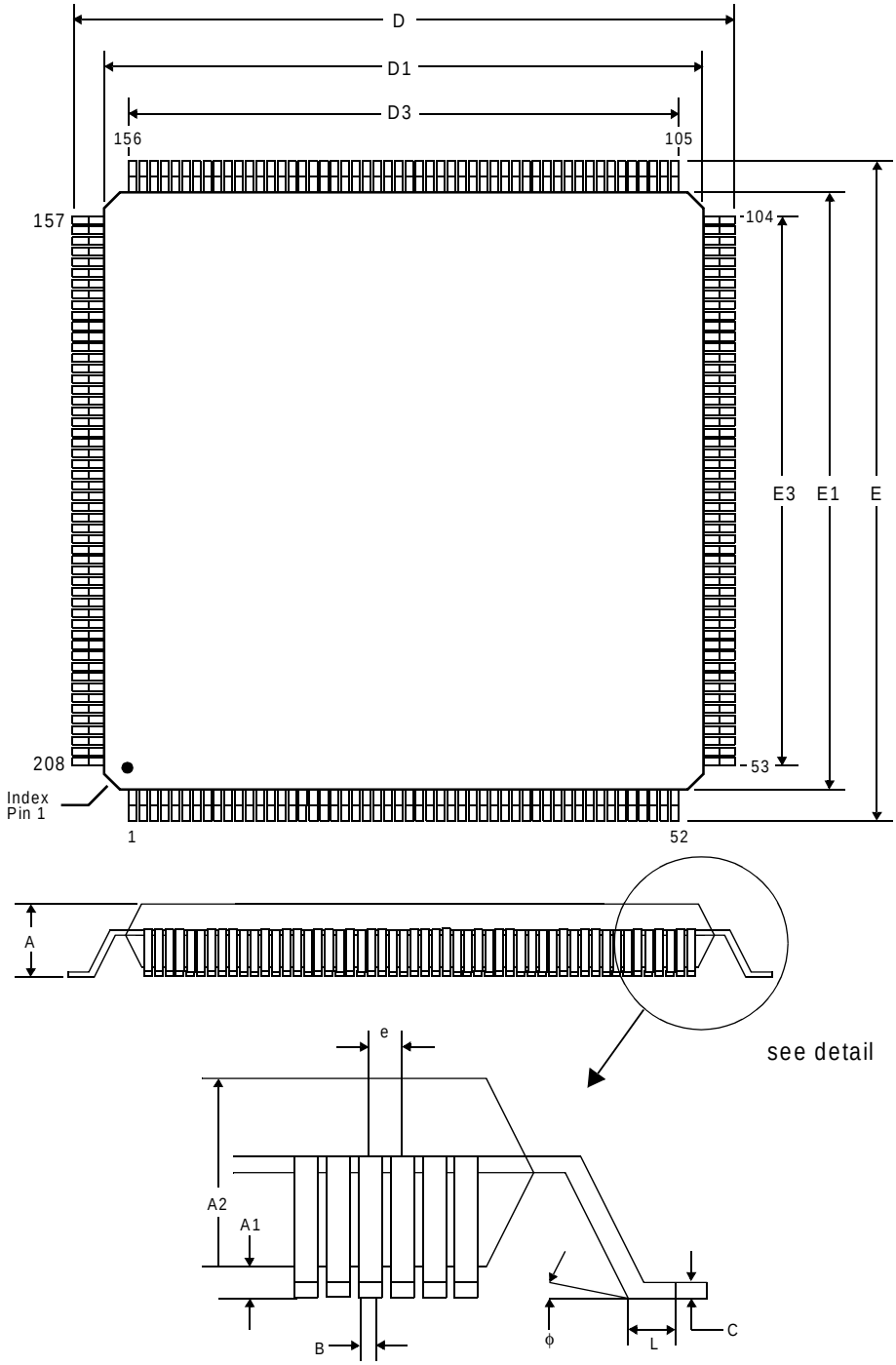
Table 8 Clock Timings

Symbol		Parameter	Min	Typ	Max	Units
t1	t_{CLK_P}	Clock period	30		100	ns
t2	t_{CLK_LT}	Clock low time	24		–	ns
t3	t_{CLK_HT}	Clock high time	24		–	ns
t4	t_{CLK_RT}	Clock rise time	–		6	ns
t5	t_{CLK_FT}	Clock fall time	–		6	ns
t6	t_{PCLK_P}	Pixel clock period	33		–	ns
t7	t_{PCLK_LT}	Pixel clock low time	15		–	ns
t8	t_{PCLK_HT}	Pixel clock high time	15		–	ns
t9	t_{PCLK_RT}	Pixel clock rise time	–		4	ns
t10	t_{PCLK_FT}	Pixel clock fall time	–		4	ns
t11	t_{ACLK_P}	Audio clock period	54		–	ns
t12	t_{ACLK_LT}	Audio clock low time	21		–	ns
t13	t_{ACLK_HT}	Audio clock high time	21		–	ns
t14	t_{ACLK_RT}	Audio clock rise time	–		6	ns
t15	t_{ACLK_FT}	Audio clock fall time	–		6	ns
t16	t_{TDMCLK_P}	TDM clock period	62.5		–	ns
t17	t_{TDMCLK_LT}	TDM clock low time	25		–	ns
t18	t_{TDMCLK_HT}	TDM clock high time	25		–	ns
t19	t_{TDMCLK_RT}	TDM clock rise time	–		6	ns
t20	t_{TDMCLK_FT}	TDM clock fall time	–		6	ns
PCLK2XSCN (2x Pixel Clock) Timing						
t7	t_{PCLK_LT}	Pixel clock low time	15		–	ns
t8	t_{PCLK_HT}	Pixel clock high time	15		–	ns
t9	t_{PCLK_RT}	Pixel clock rise time	–		4	ns
t10	t_{PCLK_FT}	Pixel clock fall time	–		4	ns

Table 8 Clock Timings

MCLK (Audio Clock) Timing						
t11	t_{ACLK_P}	Audio clock period	54		–	ns
t12	t_{ACLK_LT}	Audio clock low time	21		–	ns
t13	t_{ACLK_HT}	Audio clock high time	21		–	ns
t14	t_{ACLK_RT}	Audio clock rise time	–		6	ns
t15	t_{ACLK_FT}	Audio clock fall time	–		6	ns
Video Timing						
	Symbol	**Parameter**	**30 MHz**			**Unit**
			Min	**Typ**	**Max**	
t21	t_{PCLK_ST}	PCLKQSCN setup time to PCLK2XSCN	6		–	ns
t22	t_{PCLK_HT}	PCLKQSCN hold time to PCLK2XSCN	2		–	ns
t23	t_{S_STPCLK}	Syncs setup time to PCLK2XSCN	6		–	ns
t24	t_{S_HTPCLK}	Syncs hold time to PCLK2XSCN	2		–	ns
t25	t_{VS_ODT}	Video data and syncs output delay time to PCLK2XSCN	4		12	ns

MECHANICAL DIMENSIONS



Note:
1. All dimensions are in inches (millimeter).
2. Actual package used has millimeter native dimensions – take care with rounding from metric to imperial.

Symbol	Min	Nom	Max
A	–	–	0.165
A1	0.010 (0.25)	–	–
A2	0.130 (3.30)	0.134 (3.40)	0.138 (3.50)
B	0.007 (0.18)	0.009 (0.23)	0.011 (0.28)
C	0.005 (0.12)	0.006 (0.16)	0.008 (0.20)
D	1.195 (30.35)	1.205 (30.60)	1.215 (30.85)
D1	1.098 (27.90)	1.102 (28.00)	1.106 (28.10)
D3	1.004 (25.50) REF		
e	0.0197 (0.50) BASIC		
E	1.195 (30.35)	1.205 (30.60)	1.215 (30.85)
E1	1.098 (27.90)	1.102 (28.00)	1.106 (28.10)
E3	1.004 (25.50) REF		
L	0.016 (0.40)	0.020 (0.50)	0.024 (0.60)
ϕ	0 i	2.5 i	5.0 i

Figure 25 208-pin Plastic Quad Flat Package (PQFP)

SAMPLE SCHEMATICS

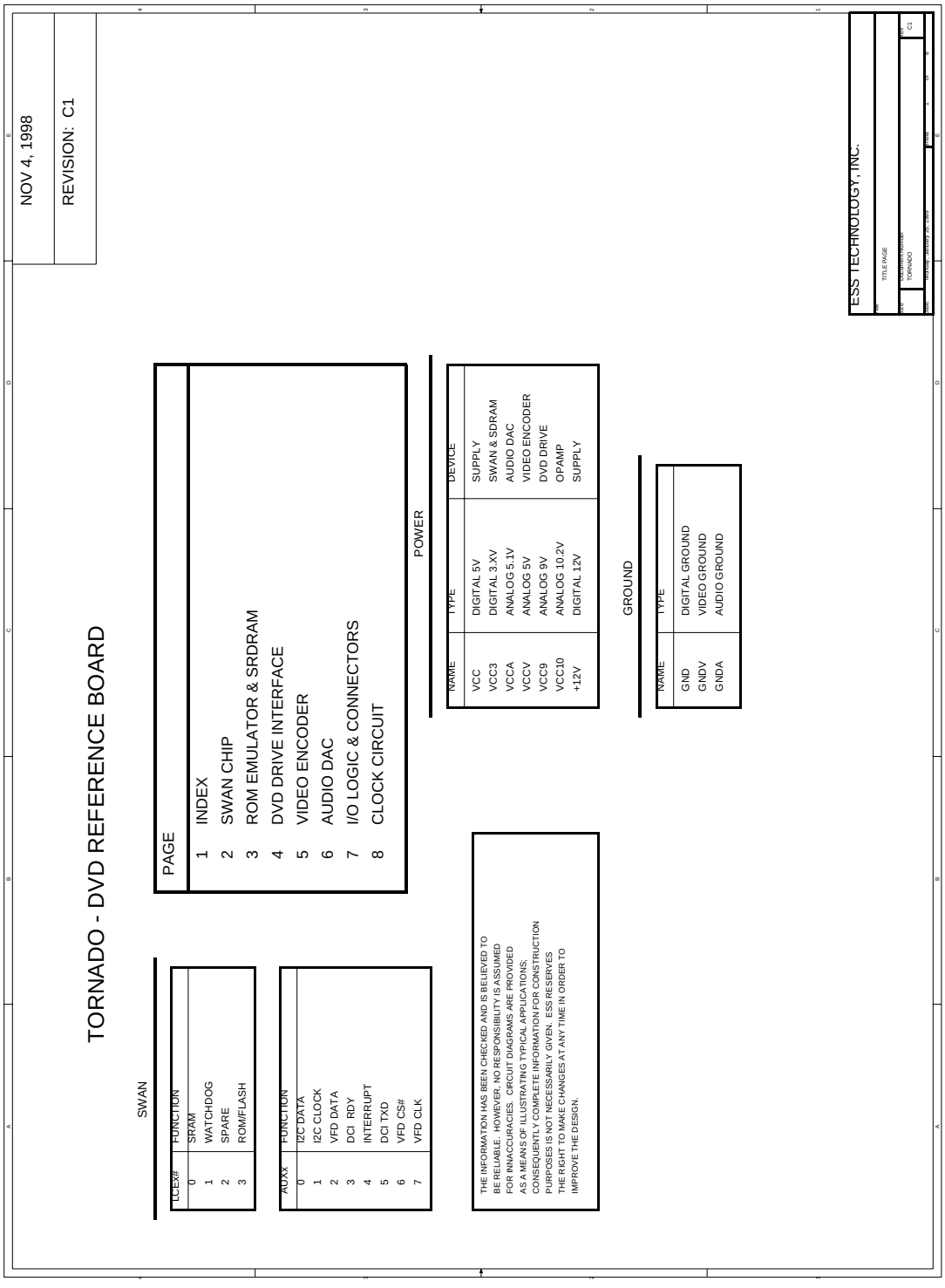


Figure 26 Schematics Index

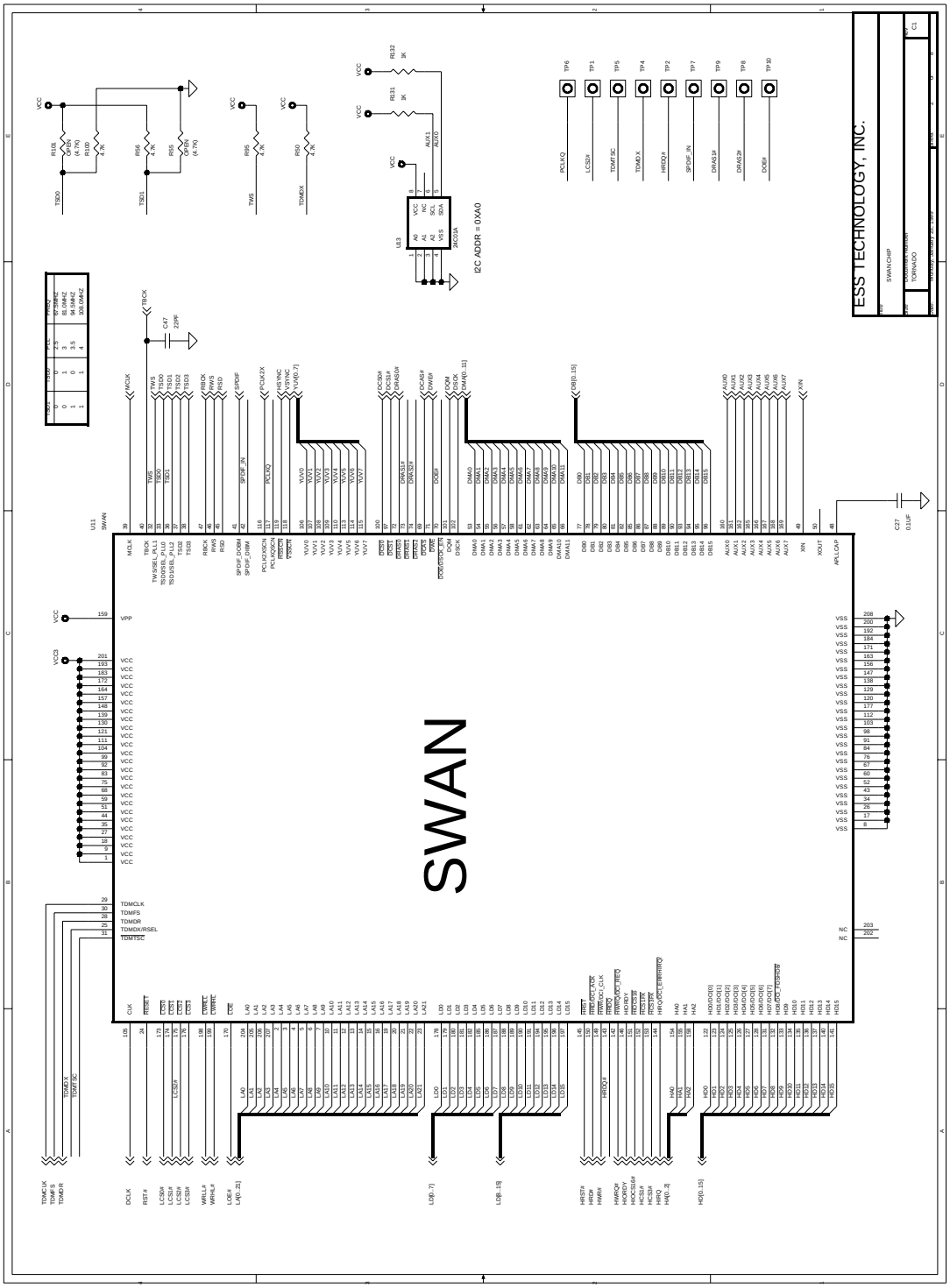


Figure 27 Swan-2

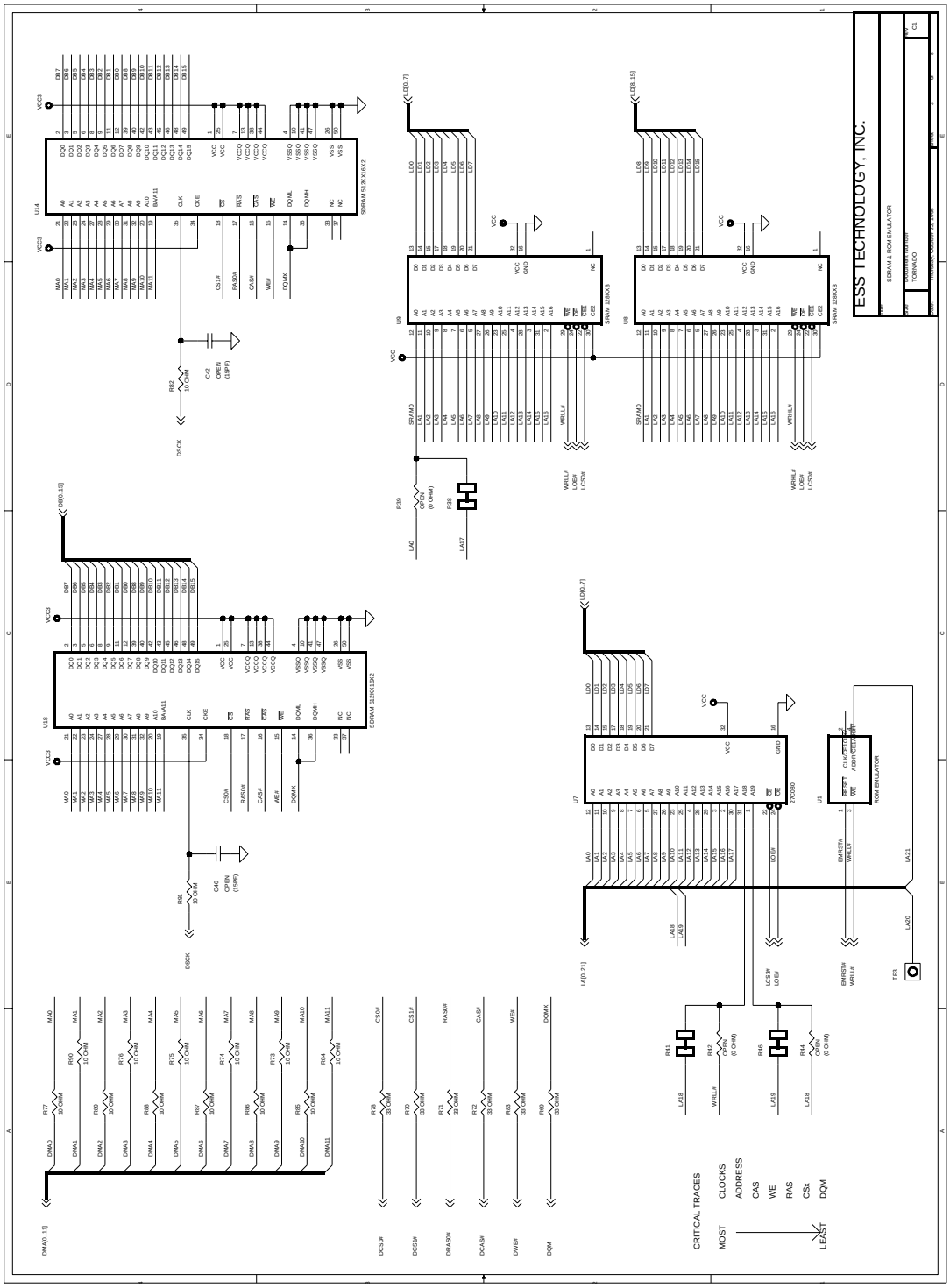


Figure 28 Memory

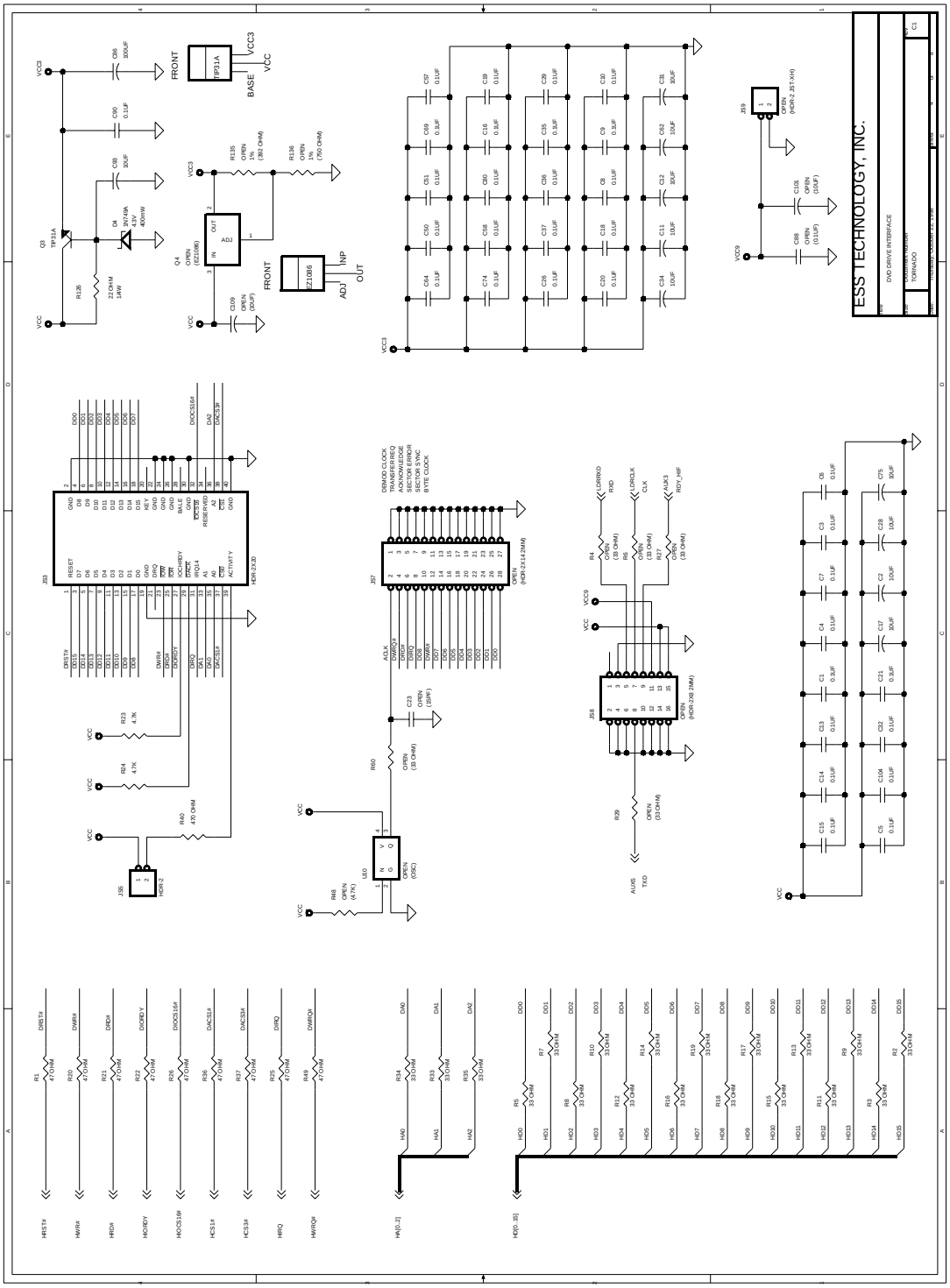


Figure 29 Drive

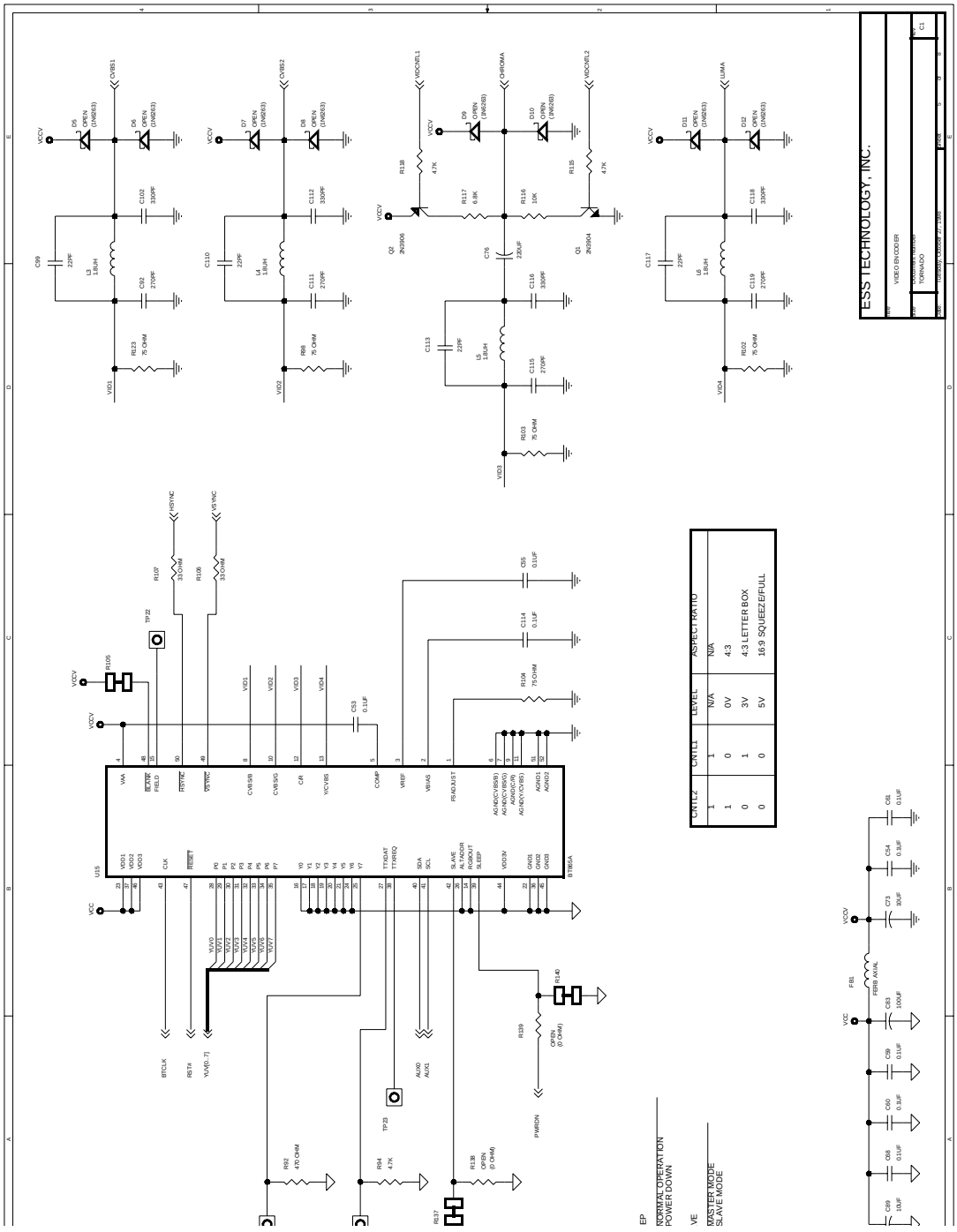


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Figure 30 Video

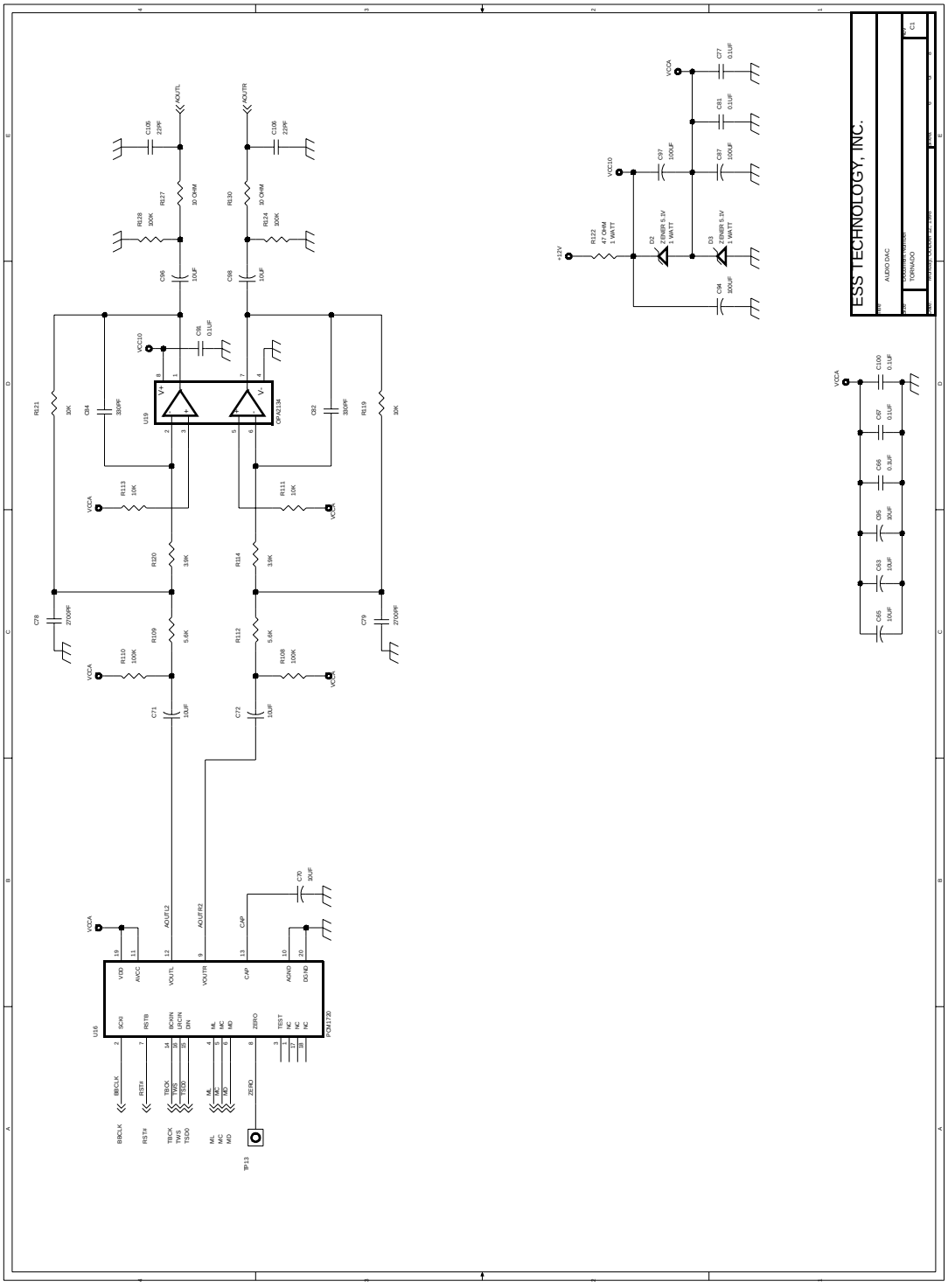


Figure 31 Audio

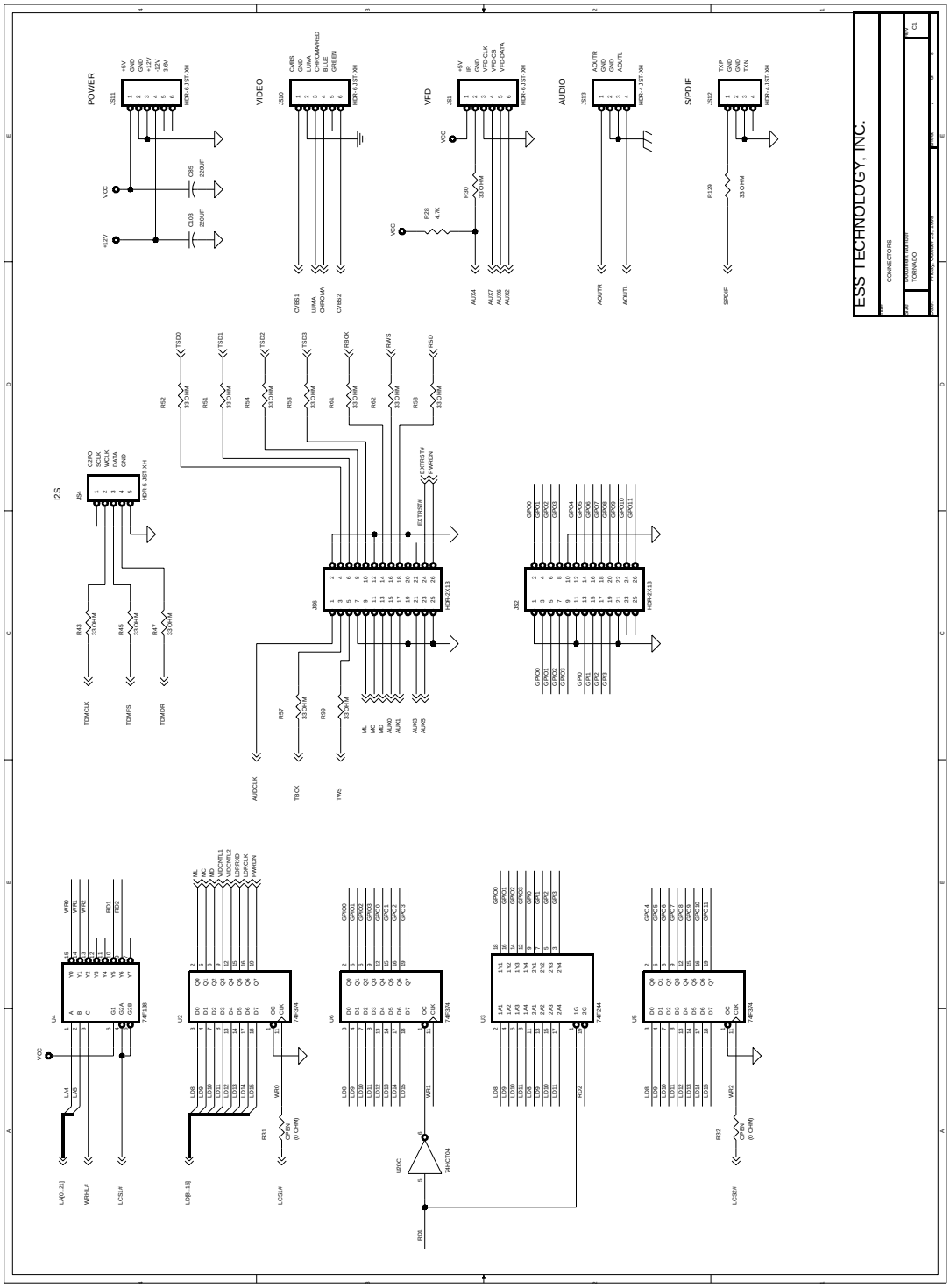


Figure 32 Connectors

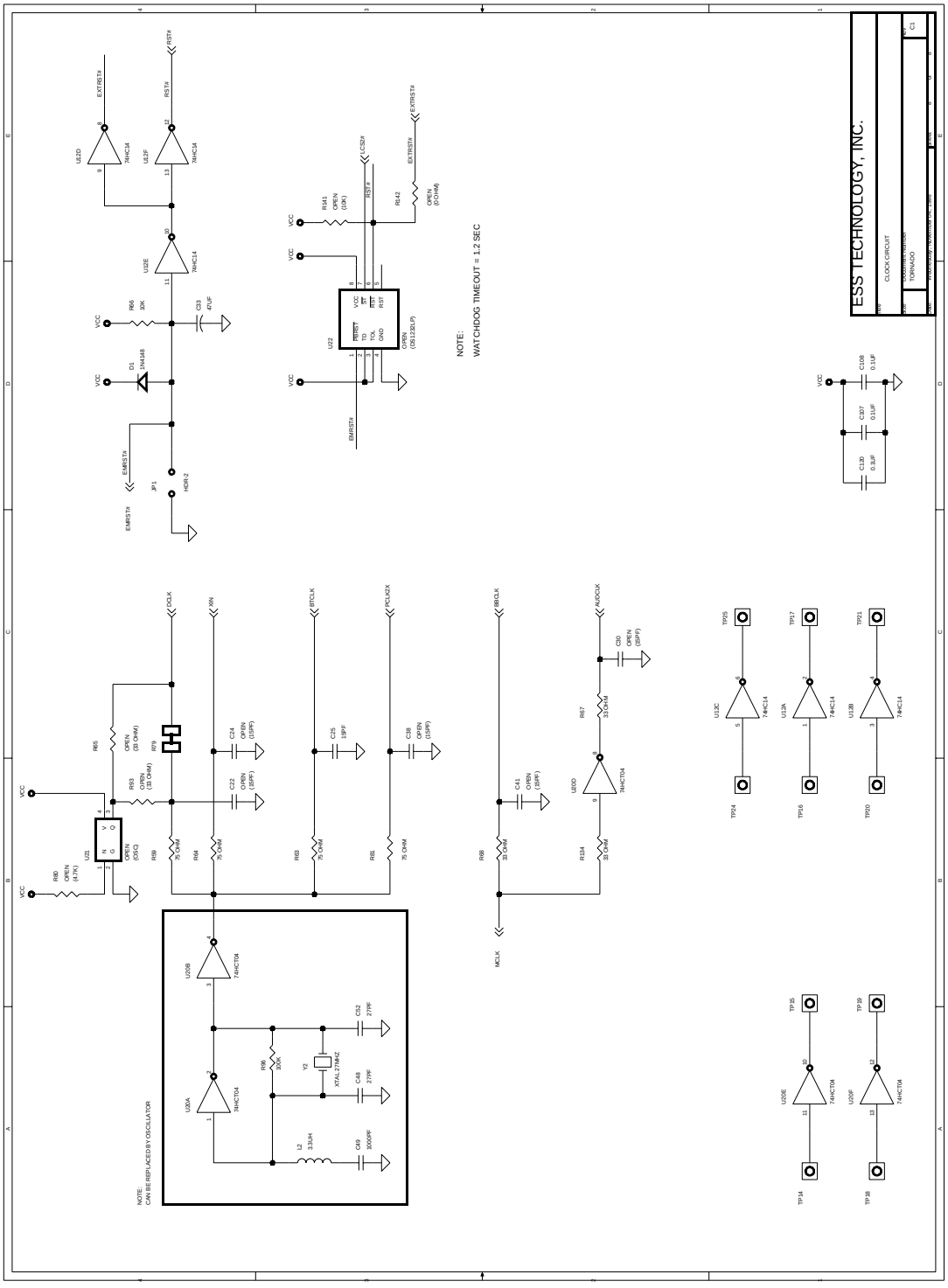


Figure 33 Clock

APPLICATION NOTES

Application Note

VideoDrive® Processor Chip Swan-2 Family #101

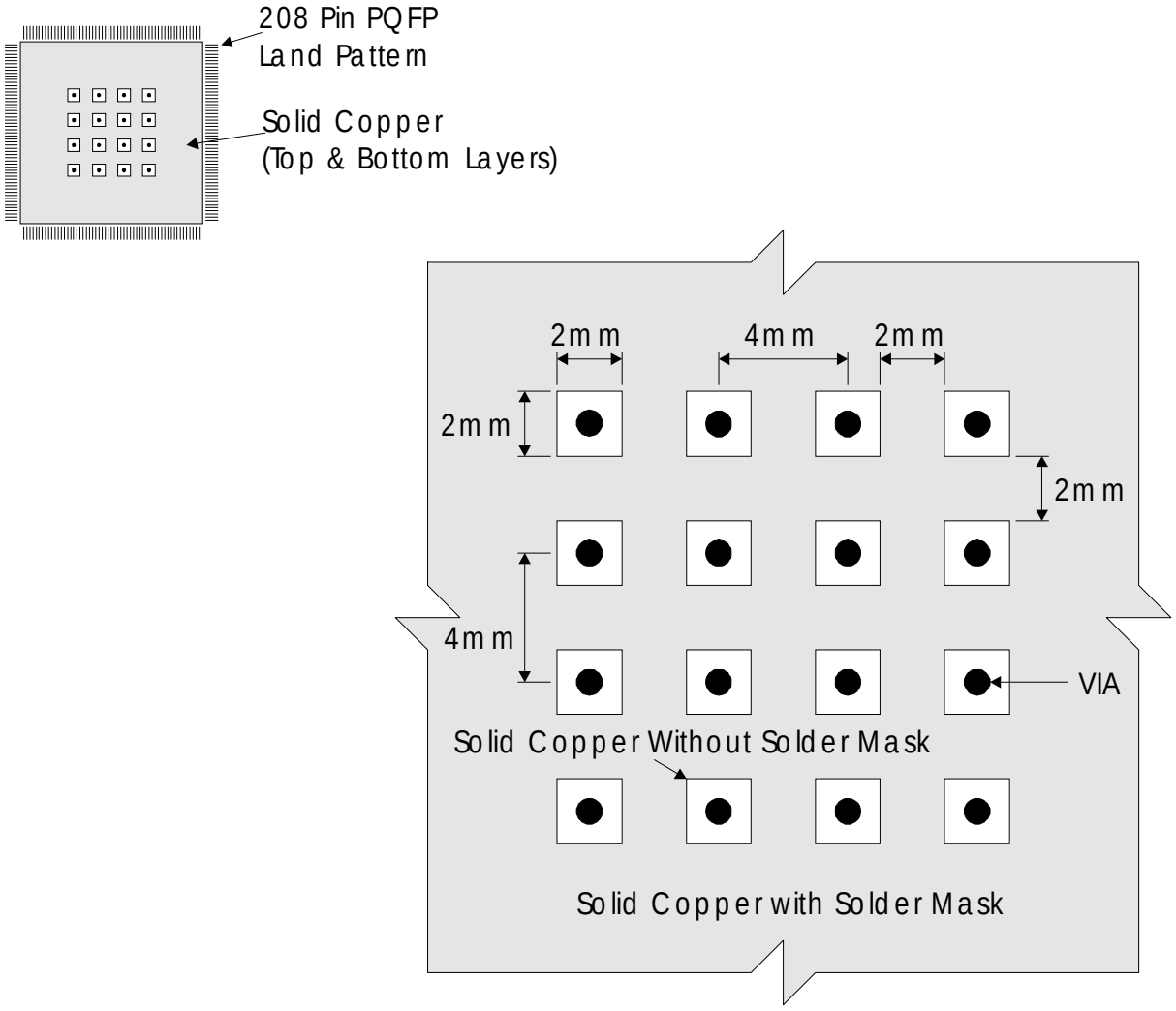
Date : September 17, 1998
Subject :

PCB Layout Consideration Regarding Heat Dissipation

1.0 Recommended Printed Circuit Board Layout

The Swan-2 family of processor chips need additional heat sinking. To accomplish this in an economical manner, the following PCB layout is recommended.

The land pattern for the Swan-2 chips still use the standard 208 pin PQFP footprint. Addition of a solid copper fill on the top and bottom layers, along with 2mm square solder mask exposures and via holes in the center of each exposure is recommended.



Application Note
4108-2

ES4108/4208/4308/4408 Swan-2™ Processor Chip
Changes in Pin Description section of ES4108/4208/4308/4408 Data Sheet

Subject :

Pin 159: Peripheral Protection Voltage

The following is a correction to the current ES4108/4208/4308/4408 Data Sheet. The current VPP definition in the ES4108/4208/4308/4408 Pin Description section (p. 4) is:

VPP	159	I	5V digital power supply.

This is now revised as follows

VPP	159	I	Peripheral protection voltage.[1,2]

1. VPP is not necessary at 5V. VPP should always be:

VDD <= VPP <= 5.5V

2. The VPP range is determined by the highest voltage of all digital parts that are connected to the ES4108/4208/4308/4408.

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